RCA

Broadcast Equipment

Maintenance

For High Band Television Tape Machines

TR-3 MI-43232
TR-4 MI-43233
TR-22 MI-43234
TR-50 MI-43301-HB

IB-32140

Broadcast Equipment

Maintenance

For High Band Television Tape Machines

TR-3 MI-43232
TR-4 MI-43233
TR-22 MI-43234
TR-50 MI-43301-HB

Commercial Electronic Systems Division/Front and Cooper Streets/Camden, New Jersey, U.S.A., 08102

Printed in U.S.A.—PP649

IB-32140

TABLE OF CONTENTS

GENERAL DESCRIPTION

MODULE CIRCUIT ANALYSIS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

GENERAL DESCRIPTION

INTRODUCTION

This instruction book covers the system description, circuit description and maintenance information required to service High Band tape equipment. Included in this book are the field modified TR-3HB tape player, the compact TR-4HB tape recorder, and the deluxe, TR-22HB tape recorder and also the TR-50 tape recorder which is factory built for high band operation.

Information presented in this instruction book is divided into two parts. The first part is the System Description, which describes the functions of the video and FM system. The description is intended to quickly orient the serviceman so that he may better understand the main signal paths throughout the modules and to what extent the signals are processed.

Reference should be made to the diagram book pertaining to your equipment for complete schematic and assembly diagrams of the machine. In addition, at the back of the diagrams book there are several functional diagrams which are used when discussing the video and FM system description.

The basic operation of the Monochrome ATC, color ATC, and the video processing system, have not been altered by the high band modification. However some circuit modifications have been made, and it is only these differences which will be covered in this book. Therefore, the functional diagrams of the ATC systems, found in the diagrams book, and the video processing system, found at the rear of this instruction book, will be used when describing these changes.

The second part of the book covers Module Descriptions. These describe the circuits contained in each module. Adjustment procedures are included for the module following their circuit descriptions.

Table 1 presents a list of modules that are used in the several high band machines grouped according to their function. Pertinent information, such as module number, descriptive name of module and master item number used to order the module may also be found in table 1.

TABLE 1—HIGHBAND MODULES

Module Name	*Symbol*		*Master Item No.*	
	TR-22	*TR-3/4/50*	*TR-22*	*TR-3/4/50*
Record System				
Video Input	H103	HA1	43268	43270
Modulator	H203	HA3	35916	35916
Modulator AFC	H204	HA4	35915	35915
FM Reference	H205	HA5	43274	43274
Record Amplifier	H118	HA2A2	43279	43279
Record Switch	H206	HA6	43278	43278
Playback System				
FM Preamplifier	H116	H2A1	43254	43254
Playback Amplifier	H212-13	HA11-12	43255	43255
FM Switch	H214	HA13		43213
FM Equalizer/Filter	H215	HA14	43256	43256
Demodulator	H217	HA16	43257	43257
Demodulator Output	H219	HA18		43218
Signal Processing				
Video Processor	H131	HA21	43206	43204
Video Output	H132	HA22	43207	43205

TABLE 1—HIGHBAND MODULES (Continued)

Module Name	*Symbol*		*Master Item No.*	
	TR-22	*TR-3/4/50*	*TR-22*	*TR-3/4/50*
Miscellaneous				
Coupling Kit	H233			
Power Supply	H1A10	H1A10	43258	43258
Standards Gen	H220	HA19		
Regulator	H329	HC20		
Preamplifier Filter	H119	H2A9	43231	43231
DOC AGC*	H218	HA17		
DOC*	H216	HA15		

* Accessories

NOTE: In most cases, the descriptions contained in this manual pertains to all machines, unless specifically mentioned otherwise.

SYSTEM FUNCTIONAL DESCRIPTION

Record Path

(Refer to figure 52 in IB-32114 for TR-3HB/4HB machines; figure 49 in IB-32143 for TR-22HB machines; figure 93 in IB-31807 for TR-50 machines.)

Composite video from the VID IN jack 6J1 or 12J1, is supplied to the Video Input module and may be observed at TP1. The video signal is fed to the input control circuits. These controls are selected by the position of the UNITY-VAR switch. With the switch in the UNITY position, a gain of one is maintained through the module to the outputs. This switch position is used under normal circumstances with a standard signal in which no modification of characteristics is required of the signal. Thus, with one volt input, one volt is supplied to the output of the module.

If the input signal departs from standard amplitude or frequency response, the UNITY-VAR switch is positioned to VAR and amplitude alterations are made with the VIDEO LEVEL potentiometer, R6 and response compensation is made with the HF COMP potentiometer, R18. Under this condition, the module gain may not be unity because one volt peak-to-peak is always required at the output and the controls are set accordingly to produce this required output.

Two parallel outputs are supplied from the amplifier stage. One path produces an output to the CRO waveform monitor, picture monitor and the modulator AFC module. In the main signal path, the video is applied to the wide band or narrow band filters that are selected by the machine operating standard. The filters have characteristics in which their cutoff frequency is high enough to have no affect on the signal, yet is low enough to remove high frequency noise and undesired high frequency video accompanying the input signal.

After filtering, video is supplied to the pre-emphasis network containing RC circuits that are selected for each standard by the standards switch. The network emphasizes the high frequencies to improve the signal-to-noise ratio, and provides a flat attenuation which is controlled to supply correct drive and modulation level (deviation) for the Modulator module.

Pre-emphasized video is supplied to the Modulator module where it may be observed at TP1. The video is coupled through the DEVIATION control and the normally closed contacts of relay K1 to the video driver stage. The driver splits the signal and supplies two channels which are each clamped separately to a dc reference voltage to establish a blanking frequency.

The Modulator converts video to FM, thus the modulation frequency depends on the video level. This means that black on the video signal produces one frequency limit, while white produces the other frequency limit, and the greys produce a range of frequencies within these limits. The clamp circuit establishes the basic reference frequency (blanking).

The clamp drives two voltage controlled oscillators in the 100 megahertz region so that when the voltage on the video signal goes toward sync tip, the low frequency oscillator frequency increases, and the high frequency oscillator decreases. Both oscillators supply their outputs to a mixer stage to extract the difference frequency between the oscillators. This mixer difference frequency is in accordance to a range determined by the selected operating standard.

The difference frequency supplied from the mixer stage is amplified and fed out of the module in two paths. One output is to the Modulator AFC module which is part of the AFC loop and holds the FM to the correct blanking frequency. The second output is to the Record Switch module.

The Modulator AFC module receives video from the Video Input module and feeds it to a sync separator circuit. Separated sync, which is observable at TP2, is supplied to the FM Reference module where it keys the white insert logic and on to the Reference Generator module which is the record sync, reference. Another output from the sync separator circuit is fed internally to a sample pulse generator circuit which causes a pulse to be formed during the back porch interval to control an electronic switch.

The electronic switch circuit receives the black reference frequency from the FM Reference module, and FM from the Modulator module. Principally, the output from the switch is the standard black frequency except during the back porch interval when it is FM from the Modulator module.

The switch circuit output is supplied to a limiter circuit and then to a frequency demodulator circuit that supplies a dc voltage level during the sampling interval in relation to the difference between the black reference frequency and the FM frequency corresponding to the back porch video level. With no frequency error, the demodulator circuit supplies no output. However, if a frequency error exists in the black level, the output during the sample pulse time will be different than the remaining output. This is the AFC error pulse that is supplied to the Modulator module for error correction.

The sample pulse produced during the back porch interval from the sample pulse generator is supplied to a clamp pulse generator circuit. The clamp circuit in the Modulator module is driven by balanced positive and negative pulses supplied from the clamp pulse generator circuit in the Modulator AFC module. The AFC error pulse (if present) from the demodulator circuit has an amplitude which is proportional to the error in the FM black level frequency. The error pulse is supplied to the clamp circuits in the modulator module and upsets the balanced dc voltage which causes the FM carrier to shift to the correct frequency.

The AFC error pulse is also supplied to the AFC error detector circuit. Sampling is accomplished with the pulses that are identical to the positive and negative pulses supplied to the clamp in the Modulator module. If an error exists, the resulting dc voltage is amplified and used to energize a relay that illuminates the FM FREQ warning indicator. This indication warns the operator that the carrier frequency error is excessive.

The E-E control switch is located on the front panel of the Modulator AFC module. When this switch is in the OFF position, the E-E control bus is disabled. Also, in this position the E-E OFF indicator (TR-22HB only) illuminates whenever the machine is in STANDBY, WIND or STOP modes. When the E-E switch is in the ON position, the E-E bus is activated and operates relay K2 in the FM Reference module and relay K3 in the FM Equalizer module.

The energizing of relays K2 of the FM Reference module and K3 of the FM Equalizer module sets up a back to back or electronic-to-electronic FM system. The input video is converted to FM as previously described and follows the circuit path as it would to be recorded. However in the E-E path the signal is diverted in the Record Switch module to the FM Reference module and to the FM Equalizer module in the playback system. The signal is now processed as if it were a signal from tape in a playback mode. The FM is demodulated to video and passes on through to the output of the machine. This path when energized gives a continuous check on the machines record and playback system. This E-E path is disabled when the machine is in playback.

The FM Reference module provides precision standard frequencies corresponding to white, black and gray levels in video signals. These standard frequencies are in accordance with the operating standards. The white frequency corresponds to the peak white frequency required from the Modulator module. A resistor matrix controlled by the operating standards supplies a dc voltage level to the Modulator which establishes approximate blanking (back porch interval) level. The blanking frequency is then held to exact frequency by the Modulator AFC module by the AFC loop.

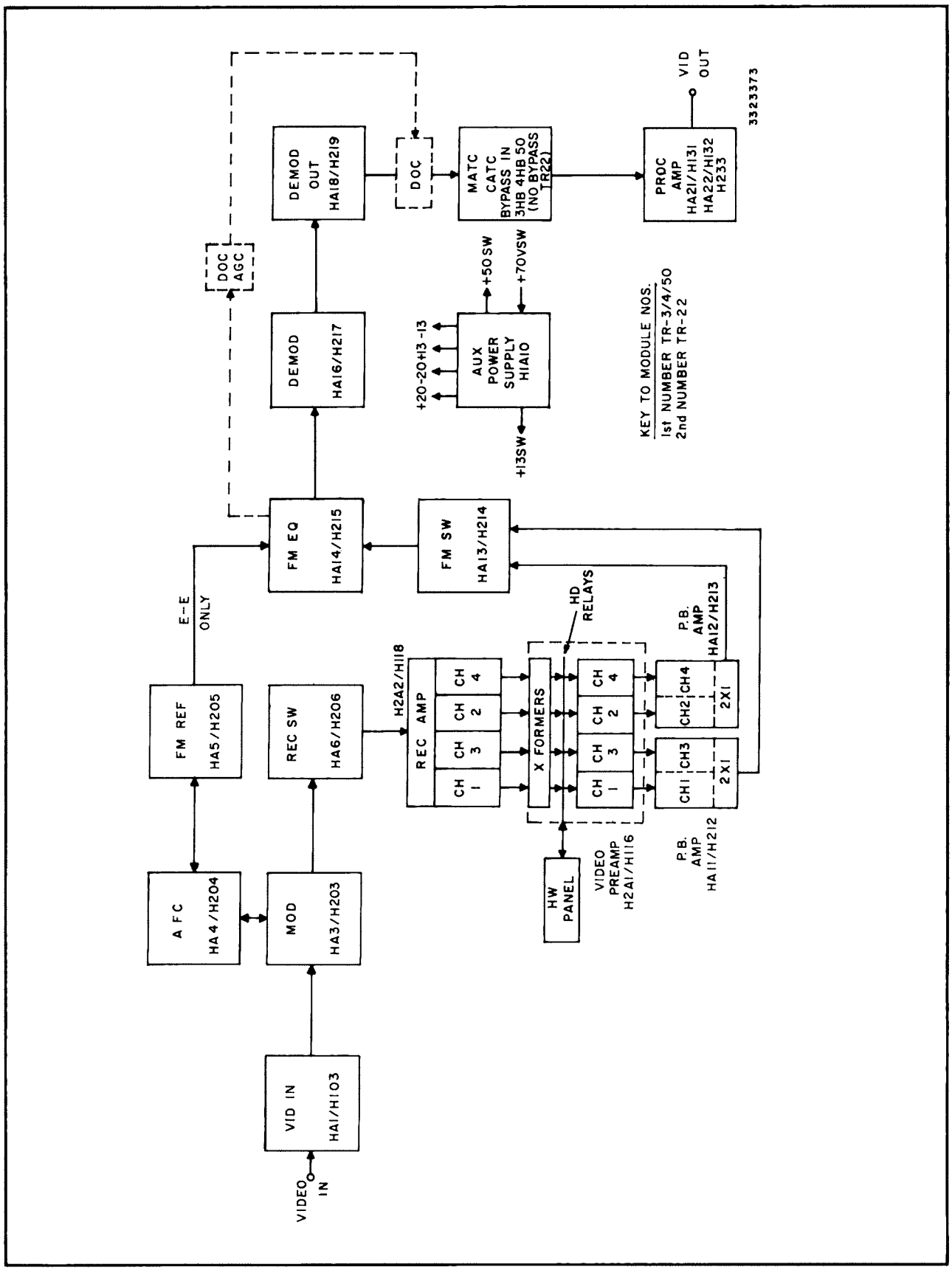
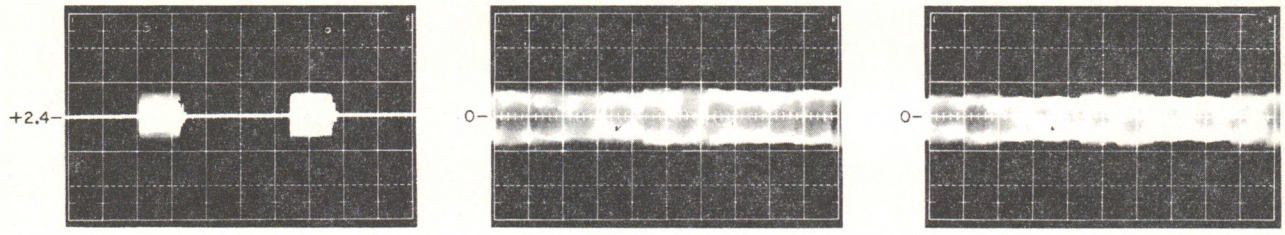


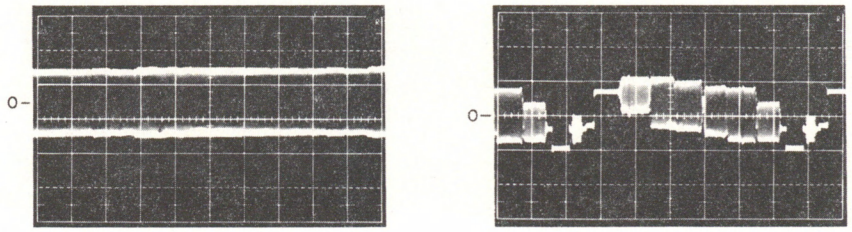
Figure 1—TR-3/4/22 Highband Conversion Block Diagram and Typical Waveforms



A. TP1, P.B. Amp.
0.1 v/cm
1 ms/cm

B. TP1, FM switch
0.2 v/cm
1 ms/cm

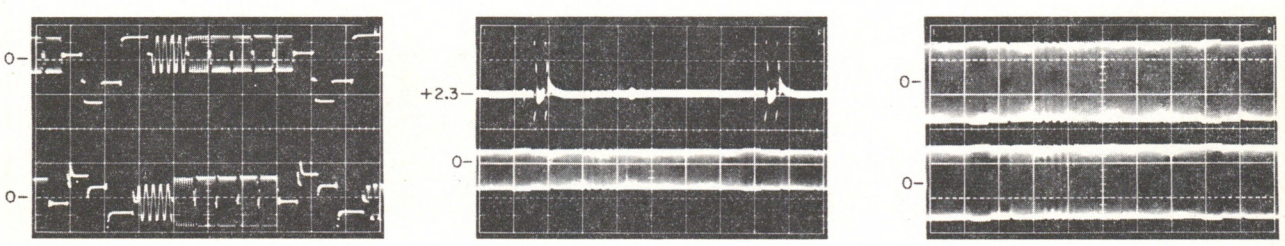
C. TP1, FM equalizer
0.2 v/cm
10 μs/cm



D. TP1, Demodulator
0.5 v/cm
10 μs/cm

E. TP1, Demod Out
0.5 v/cm
10 μs/cm

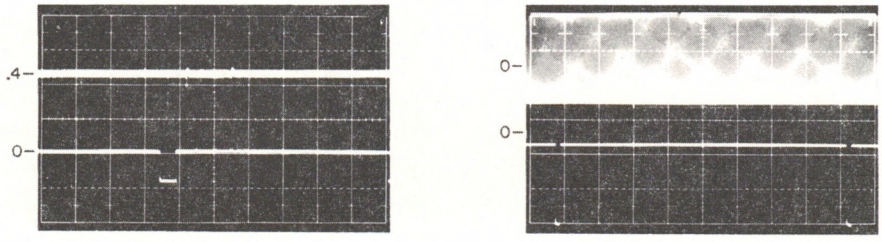
PLAYBACK PROCESS. Machine in PLAY mode.



F. Top: TP1 Video Input, 0.5 v/cm
Bottom: TP1 Modulator,
1 v/cm
Both: 10 μs/cm

G. Top: TP2 Modulator, 1 v/cm
Bottom: TP1 Rec. Sw.
0.2 v/cm
Both: 10 μs/cm

H. Top: TP2 Rec. Sw. 0.1 v/cm
Bottom: TP1 Rec. Amp.,
0.2 v/cm
Both: 10 μs/cm



I. Top: TP1 FM Ref., 0.2 v/cm
Bottom: TP2 FM Ref., 5 v/cm
2 ms/cm

J. TP2 Mod. AFC, 5 v/cm
10 μs/cm

RECORD PROCESS.. Machine in SETUP mode.

Figure 1—TR-3/4/22 Highband Conversion Block Diagram and Typical Waveforms (Continued)

In another function of the FM Reference module, noise test control is generated by pressing the NOISE TEST pushbutton. Thus, energizing a relay (K6) which in turn switches relay K3 setting up the resistor matrix in the FM Reference module, turns the gray oscillator on, and opens the preemphasis filter in the video input module to interrupt the input video path. The noise test signal may be used for video head optimization and for evaluation of recorder signal to noise performance. When in the noise test condition, the TEST indicator is illuminated. To disable the test mode, operate the STOP button.

The FM Reference module also contains the circuits and logic for the white insert pulse. This is a FM carrier equivalent to peak white for the standard in which the machine is operating. It is timed to appear during the vertical interval of the video signal. When viewed on the CRO (DEMOD OUT position), it appears as a few positive pulses, the tops of which denote the upper limit of the white peaks of video. These levels are used to set the modulator deviation on incoming video, and also check a playback to see if it was recorded at the proper levels.

White insert is accomplished by pushing the white insert pushbutton on the Record Switch module, and remains on as long as the button is pressed. The circuit is inoperative at all other times. White insert pulses are never recorded on the tape.

The FM Reference module also houses the dc record level controls for channel #1 and #3.

FM from the Modulator module is coupled through the normally closed contacts of relay K1 in the Record Switch module. When rf copies are being made, the relay is energized by the RF COPY control, a front panel selector switch on the FM Equalizer module, and the rf copy input to the machine is obtained from an auxiliary TV tape machine operating in the PLAY mode. The RF COPY LEVEL control permits the input level to be set correctly.

After passing through the contacts of relay K1 and being amplified, the FM signal takes two paths. The main signal path is to the splice gate circuit which is an electronic switch that is controlled by the splice circuitry in the machine. If this accessory is not in the machine, the FM signal passes through an amplifier stage and is then supplied to the Record Amplifier module.

The alternate FM signal path is the beginning of the E-E FM signal path. The E-E signal is amplified prior to being supplied to the FM Reference module. To this is added the white insert pulses from the Record Switch module to form the E-E FM and white insert signal.

FM from the Record Switch module is supplied to the Record Amplifier module. The signal is amplified and passed through a CSEF stage that provides an output to drive the four separate record channels. The level controls, located on the FM Reference Module and the Record Switch module, permit the FM level supplied to the heads to be set for optimum current through record transformers located in the pre-amplifier module.

Each record transformer output is coupled to the headwheel through the energized head transfer relays. The ground returns for each head on the headwheel are connected to a common lead through a current transformer to ground in the pre-amplifier module. The current transformer output in the TR-22HB is supplied to the indicator module. When the head current is less than a preset value, the red HD-1 indicator lights.

Playback Path

(Refer to figure 52 in IB-32114 for TR-3HB/4HB machines; figure 49 in IB-32143 for TR-22HB machines; figure 93 in IB-31807 for TR-50 machines.)

The playback signal extracted from tape via the heads passes through the normally closed contacts of relays K101, K201, K301, and K401 in the FM pre-amplifier module. These relays are de-energized during playback.

The first two stages of the pre-amplifier module are a feedback pair. The pair are designed for low input impedance and flat frequency response. The low input impedance eliminates the need for adjustment of head resonance.

Three feedback amplifiers follow and provide sufficient amplification to drive the Playback module. These feedback amplifiers function only during playback. This is controlled by the +13 volt switched potential. Thus in any mode except playback the amplifiers are completely disabled, thereby eliminating crosstalk. The control relay for the +13 volt switched potential is in the Regulator module.

The four playback channel outputs from the FM Pre-amplifier module are supplied to two identical dual channel Playback Amplifier modules. The odd numbered channels are supplied to one module and the even numbered channels to the other. The input of each channel is passed through a GAIN control and may be observed at a test point.

Equalization of the playback FM signal is provided by the use of a cosine equalizer circuit which maintains a constant group delay so that it does not alter the original phase relationship of the FM signal frequency components. The amount of equalization is controlled by the front panel PB EQUAL potentiometers.

The two playback channels contained in each Playback Amplifier module are combined into one output by a coarse 4 × 2 switcher. The pulse drive for this switching is obtained from the FM Switcher module.

Each Playback Amplifier module supplies a single output. The outputs from the two playback amplifiers are supplied to the FM Switch module and are fed in parallel to a precision switching circuit. The sequential output of channels 1 and 3, and 2 and 4 from their respective gates are combined in the electronic switch circuit on the FM Switch module to form a single output.

Timing to activate the coarse switches in the Playback Amplifier module is controlled by the tonewheel pulse which triggers a 240-hertz multivibrator. The multivibrator supplies one output directly to the coarse gate that switches channels 2 and 4. Another output from this multivibrator is delayed, and the delayed pulse triggers a 240-hertz multivibrator used for coarse gate switching channels 1 and 3. The delay corresponds to one complete head scan thus placing channel 3 information immediately following the completion of channel 2 passage through the opposite gate.

Composite playback FM in the FM Switch module is produced by the precision switch which is activated by the 4XTW pulse timed to the horizontal AFC sync pulse. This timing for precise switching is controlled by a series of gates that must have correct starting points before they are activated. Switching between the precision quads takes place at the time of the first AFC sync pulse interval occurs during the period when two heads overlap in reading information from the tape. To confine the switching to the overlap region, a delayed 4XTW pulse is developed in the Tonewheel Processor module. The 4XTW pulse resets the 960 hertz multivibrator. The first AFC sync pulse then sets the multivibrator, and the other sync pulses have no effect on the stage until another 4XTW pulse resets the multivibrator gate. The gate output triggers a divide-by-two switch-control multivibrator which has been enabled by the tonewheel pulse. Thus, the driver amplifier feeds the precision switch with positive and negative control pulses that are keyed with related timing sequences.

The video from the switching circuit is amplified, filtered and supplied to the FM Equalizer module. The filter has high-pass characteristics that remove the low frequency components normally present after switching which would otherwise cause "banding" in the video presentation.

In the TR-3/4/50 the unfiltered FM signal is supplied to a detection circuit. The detected FM signal is converted to a varying dc and supplied to the FM SELECT switch on the RECORD control panel for the purpose of monitoring the playback FM signal on the FM meter. In this way the operator is able to adjust CT Phase for maximum playback signal strength.

Playback FM from the FM Switch module is fed to a low-pass filter in the FM Equalizer module that removes spurious components from the signal. Filtered FM is then supplied to a stage that drives the tapped delay line that follows. As with the equalizer circuit in the Playback Amplifier modules, the sending end of the line is terminated and the receiving end is unterminated.

The delay line provides two outputs; one is directly to the difference amplifier stage that follows. The second output is also supplied to the difference amplifier. but first passes through one of five taps in the delay line and then through the front panel VERNIER EQUALIZATION control before arriving at the difference amplifier. A tap of the delay line, corresponding to a coarse adjustment, is selected by the front panel STEP EQUALIZATION switch.

The selected delay line tap determines the frequency of the response peak due to the reflection on the delay line. The VERNIER EQUALIZATION potentiometer setting changes the relative level from the delay line tap to the signal level through the delay line. These differences are combined in the difference amplifier and an algebraic sum is provided at the output. Due to the reflection on the delay line, varying amounts of constant phase response peaking are available at the difference amplifier, depending on the setting at the VERNIER EQUALIZATION control.

An amplifier stage increases the signal level supplied from the difference amplifier, and one output is supplied to the dropout compensator accessory equipment when used in the machine. The main output is supplied through relays K3 and K4 to the linear rolloff filter. During playback, relay K3 and

K4 will normally be de-energized so that the FM from the Equalizer section is applied directly to the Linear Rolloff filter. However, if the White Insert button is pressed, the relays will be energized so that the signal is diverted to the FM Reference module to add the white insert test signal, and returned to continue its normal path through the Linear Rolloff filter. In the Record or Set up modes of operation, relay K3 will be energized to accept the EE FM signal from the FM Reference module. In all other modes (WIND, STBY, STOP), relay K3 will be energized only if the EE switch is ON.

The linear rolloff filter diminishes the noise level derived from head to tape transfer of the signal without affecting the ratio of total sideband energy to carrier energy. Thus, the filter improves the signal-to-noise ratio without affecting the video information conveyed by the FM sidebands and carrier. A choice of filters is made by activating relays K1 and K2 from the FM Standard bus. Filtered FM is amplified to compensate for losses caused by the termination resistors and supplied to the Demodulator module.

An auxiliary function of the FM Equalizer module is to supply the CRO with detected FM envelopes of the head output for monitoring the FM signal amplitude. Detected FM is chopped by an electronic switch (chopper) that is activated by the chopper drive pulse generator stage. The latter stage receives pulses at a four-times-tonewheel (4XTW) rate which causes the chopper output to short or chop the detected FM signal with each pulse. The chopper shorting pulses reduce the signal to the zero dc voltage level, allowing the amplitude of the detected FM to be checked against the zero volt reference level. Also, since the 4XTW pulses occur during head switching intervals, switching transients are removed. Chopped detected FM is then supplied to the CRO. This presentation is used to assist in adjusting the Playback Amplifier levels and the CT track for optimum playback signal.

Filtered FM is supplied to the Demodulator module where the signal is split and processed in a push-pull manner through the module. Limiter stages clip the signal to remove variations in level, and supply the push-pull FM to the discriminator stage.

Conversion of frequency variations to amplitude variations is initiated in the discriminator circuit. Effective video level is very low compared to the carrier where constant-width pulses are generated at a repetition rate corresponding to instantaneous carrier frequency. However, the filter following the discriminator partially removes these carrier components that may cause crosstalk, and supplies the push-pull video to an amplifier stage to provide the sufficient current to drive the delay line filter. The filter is designed to eliminate all frequencies above the video band and to deliver at the output a varying average dc whose amplitude changes are a function of the video input.

The video signal is amplified and supplied to the post-emphasis circuit. Depending upon the standards selected, the post-emphasis relays are energized so that the proper reactive element is inserted to increase attenuation at the high frequency end of the pass band. This causes a roll-off of the high frequencies, which, in effect, complements the boost obtained in the pre-emphasis circuit. Each post-emphasis network also has flat attenuation that compensates for differences in the demodulated video level resulting from the various deviation ranges employed. Thus the post-emphasis network restores the pass band and level to that corresponding with the original characteristics.

During rf copy operation, limited FM is coupled through relay K10 and the FM is supplied to the RF COPY OUT connector.

The limiter balance control adjusts the ac axis so that the output FM signal is clipped symmetrically. Similarly, the demodulator balance control varies the symmetry of the signal being fed into the discriminator.

The Demodulator module also contains the standard switch and control of the non-standard indicator on the indicator panel. It is lit when the mode selector switch is positioned to low band color (LB COLOR) and the line standard selection switch is in 405 or 625 standards.

The output of the post emphasis network in the Demodulator module is coupled through a DEMOD LEVEL control which adjusts the video output of the Demodulator Output module. One video output is fed to the monitor switcher for picture monitoring. Another video output is fed to the CRO switcher for waveform monitoring. Still another video output is fed to the DOC module, jumpered through an interlock and returned to the sync separator circuit in the Demodulator Output module and to the monochrome ATC system.

Separated sync is supplied to the Tape Sync Processor module and to the monochrome ATC Error Detector module.

In the TR-22 only, separated sync is supplied to the guide servo control circuit. This circuit senses the quality of the sync signal and prevents the guide servo from entering the automatic mode if sync is absent or the signal is too noisy.

The monochrome ATC system is not bypassed and always performs its function of *time correcting* the video signal to remove any geometric distortion present in the signal. The same is true for the color ATC system in the TR-22. But in the TR-3/4/50 the color ATC system may be bypassed, as seen on the conversion block diagram, figure 1.

The monochrome and color ATC system description may be obtained by procuring a copy of one of the following publications.

Monochrome ATC	
TR-22A, B, C	IB-31661
Video System	
TR-22D	IB-31621-1
Monochrome ATC	
TR-3/4/50	IB-31819
Color ATC	
TR-22/3/4/50	IB-31652 and IB-31652A

Composite video from the ATC system is supplied to the Video Processor module where it is amplified. The gain of the amplifier is controlled either locally on the front panel of the Video Processor module or from a remote control panel.

The amplified composite video is simultaneously split into a monochrome channel and chroma channel. A clamp pulse, generated in the Sync Logic module, is applied to the back porch of the horizontal interval in the monochrome channel and clamps it to −10 volts. At this point, composite blanking is added and the old blanking and sync are removed. A new pedestal level is added which also is variable from a remote control panel, if selected.

In the chroma channel, the video signal is applied to a clamp circuit which removes all information in the blanking interval when the tape recorder is in the PLAY mode. In the E-E mode, a notch in the blanking pulse allows burst from the E-E signal to pass, since regenerated burst will have a random phase with respect to the chroma signal.

The monochrome and chroma channels are recombined in the video adder. In the PLAY mode, regenerated burst is also added, but is omitted in EE. The non-composite video signal from the adder is applied to the Video Output module, where it is delayed 0.5 microseconds in order to match the delays imposed by the sync channel processing, and passes through a high frequency boost circuit which compensates for any loss due to signal handling. Chroma gain is adjustable only locally on the front panel of the Video Output module.

Composite sync from the Sync Logic module is applied to the sync adder circuits. Sync is added to the non-composite video at the output of the video line drivers. Sync gain may be varied either locally on the front panel of the Video Output module or from a remote control panel. The composite video signal is supplied to the picture monitor and waveform monitor. Composite sync may be removed from the video signal in one or all machine outputs (#1, #2 or #3), by opening the sync switches which are located in the video output module. Therefore, composite or non-composite video may be selected.

The output video signal is fed through coupling capacitors to the video out connectors on the connector board and the monitor switchers. The coupling capacitors are located on the Output Coupling module H233 in TR-22 machines and on the Video Output module board #3 in TR-3/4/50 machines.

The auxiliary power supply which was added to the machine in order to supply additional voltages required by the new high band modules, operates independent of the regular power supply. Attached to the rear frame of the tape recorder it supplies the following dc voltages: +20 volts, +13 volts, −20 volts, +13 volts switched and +50 volts switched.

Selection of the appropriate FM standard is made by means of a rotary switch. Low Band Monochrome, Low Band Color or High Band are selected by a switch on the front panel of the Demodulator module. When a standard is chosen, the video and control circuits perform the following functions:

1. Select correct high frequency boost for required pre-emphasis.

2. Set modulator blanking frequency to preset value.

3. Select correct pair of FM reference crystals.

4. Select correct high frequency roll-off for post-emphasis required to complement pre-emphasis.

5. Activate tally lights to indicate standard selected (TR-22 only).

MODULE CIRCUIT ANALYSIS

VIDEO INPUT MODULE

CIRCUIT DESCRIPTION

General

The Video Input module equalizes the input signal for deficient high-frequency response or incorrect level. Pre-emphasis is carefully added to the signal to provide a smooth high-frequency boost according to the selected operating standard. Refer to block diagram, figure 2.

In summarizing, the Video Input module performs the three following basic functions:

1. Primarily to supply pre-emphasized video to the Modulator module.

2. Supply an input signal to the monitors and auxiliary circuits.

3. Correct for non-standard input level and response.

Controls are located at the input of the module to permit adjustment of gain and response. Front-panel UNITY-VAR selector switch is positioned to UNITY for gain of unity from the input to the monitor outputs in the module. In this position, a gain trim potentiometer inside the module is positioned to precisely preset the video-input versus video-output signals for a gain of unity. Thus, a standard one-volt peak-to-peak signal at the module input appears as one volt peak-to-peak at the monitor outputs. A termination trim potentiometer is also included inside the module to adjust the input resistance for accommodating tolerances of resistances in the voltage dividers containing the gain trim and VIDEO LEVEL potentiometers.

Positioning the UNITY-VAR switch to VAR, connects the VIDEO LEVEL and H.F. COMP potentiometers. In this condition, the module may be adjusted to accept input levels between 0.5 and 2.0 volts, and to compensate for frequency response deficiencies in the range of minus 3 dB to plus 2 dB at 3.6 MHz.

Transistors Q1 and Q5 form an equalizer stage which is adjustable for low- and high-frequency response. A tunable capacitor and inductor are set to provide for flat frequency response through the entire module. Transistor Q6 is an emitter follower that provides isolation between the equalizer and the stages that follow.

The signal from Q6 takes two paths. The main signal is supplied in the Modulator path to emitter follower Q7 (described later). The secondary signal path is to the monitor and auxiliary circuits through Q8.

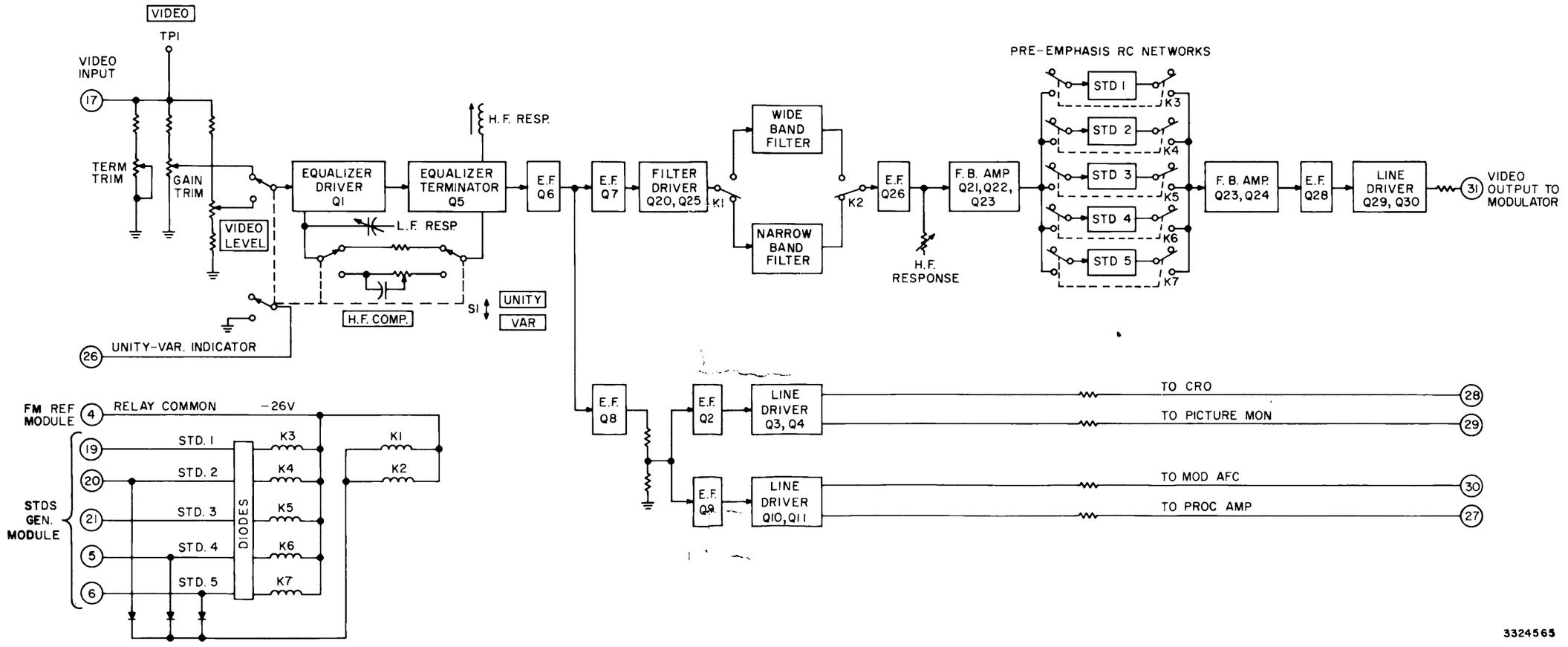
Transistor Q8 is an emitter follower that drives the voltage divider for emitter followers Q2 and Q9. This voltage divider is used to proportion the gain of the monitor channel and the Modulator channel for correct output. Thus, when the level presented on the CRO is one volt peak-to-peak, the correct level will be supplied to the Modulator module.

Transistors Q2 and Q9 are emitter followers to provide isolation between the voltage divider and the line drivers that follow. The signal from the input of Q2 to the output of line driver Q3/Q4 is unity, as is the parallel emitter follower (Q9) and line driver Q10/Q11).

Line drivers in the monitor channel (Q3/Q4 and Q10/Q11) are used to drive resistors for the sending-end terminations for the monitor channel output. Although higher gain is required from the drivers to overcome losses introduced by the resistors, reflective disturbance is overcome that might otherwise be present.

Transistor Q7 provides isolation to the filter driver circuit in the Modulator channel. Driver Q20/Q25 drives the lowpass filters at their characteristic impedance. Lowpass filters are used to eliminate noise accompanying the input signal above the useful video spectrum. These high frequency noise components might otherwise generate undesirable components during the record or playback process. Selection of either lowpass filter is with relays K1 and K2 which are positioned according to the selected operating standard. Standards selections in the Video Input module are listed in table 2.

Loading of the selector filter output is prevented with emitter follower Q26 by providing impedance isolation from the succeeding feedback amplifier stage. A potentiometer included at the emitter follower output, is adjusted to compensate for high-frequency response variations in the Modulator channel.



3324565

Figure 2—Video Input Module, Block Diagram

TABLE 2—VIDEO INPUT STANDARDS SELECTIONS

FUNCTION	*STANDARD*				
	1 *405/525* *LB Mono*	*2* *625* *LB Mono*	*3* *525* *LB Color*	*4* *405/525* *Highband*	*5* *625* *Highband*
Pin of P1 Grounded	19	20	21	5	6
Relays Activated	K3	K1, K2, K4	K5	K1, K2, K6	K1, K2, K7
Band Filter Used	Narrow	Wide	Narrow	Wide	Wide
Input Filter (Flat at MHz)	3.8	5.5	3.8	5.5	5.5
Input Filter (−3 db at MHz)	5.7	8.0	5.7	8.0	8.0
Pre-emph. (+3 db at MHz) (Note 1)	1.3	1.2	0.7	0.35	0.35
Pre-emph. (A_{HF}/A_{LF}) (Note 2)	5/1	3/1	7.56/1	2.5/1	2.5/1
Rel. LF Out (Note 3)	1.0 (Ref.)	.7	.28	1.15	.8

NOTES:

1. Frequency at which the gain is 3 dB above LF gain.
2. A_{HF}/A_{LF} is ratio of gain at frequency of maximum boost to gain at low frequency.
3. Relative outputs for standards 2 to 5 are referenced to standard 1. Absolute levels depend on Modulator sensitivity.

Feedback amplifier Q21/Q22/Q27 drives the relay terminals of the selected pre-emphasis network. A double set of contacts for separate relays is used to connect the selected RC network and provide pre-emphasis of the video signal. Selection of the correct RC network is controlled by the operating standard causing coils of appropriate relays to be energized, as listed in the table above.

The selected RC network output drives feedback amplifier Q23/Q24 through the relay contacts. The signal is then coupled through emitter follower Q28, which isolates the line driver input impedance from the high output impedance of the feedback amplifier.

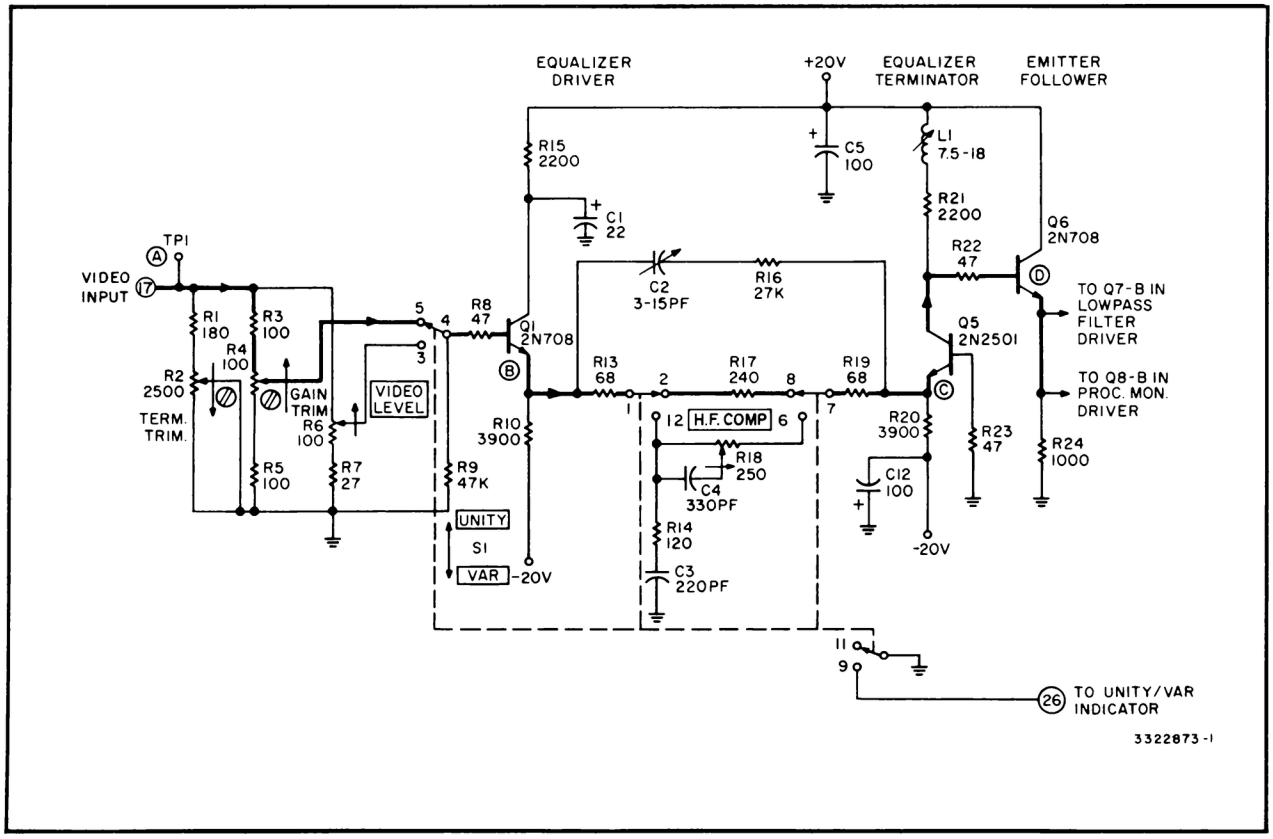
Line driver Q29/Q30 provides the Modulator channel output through a sending-end termination. This driver functions in the same manner as described for the monitor and auxiliary output drivers.

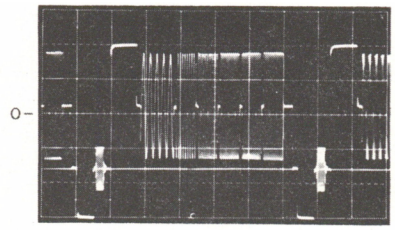
Input and Equalization

The input video signal is supplied to the Video Input module through pin 17 of plug P1 and applied to three parallel resistance branches. Resistor R1 in series with potentiometer R2 permits the input resistance of the module to be adjusted to compensate for tolerance variations in potentiometers and other resistors in the three branches. In practice, R2 is adjusted for an input resistance of exactly 75 ohms. Refer to figure 3.

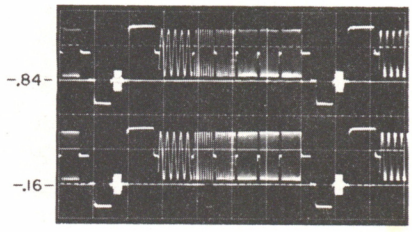
Potentiometer R4 is part of the network with range-setting resistors R3 and R5 which is used to trim the gain through the module when the UNITY-VAR switch (S1) is set to the UNITY position. Since a normal gain of unity is desired through the module from input to monitor output, the gain trim potentiometer (R4) is set to obtain one volt peak-to-peak at the module output. Under this condition, the input to Q1 is approximately 0.5 volt. The adjustment range of potentiometer R4 is not great because it compensates only for minor gain and resistance variations in the module.

Switch S1 in the VAR position places potentiometer R6, with resistor R7, into the signal path and removes resistors R3 and R5 with potentiometer R4. Potentiometer R6 is the VIDEO LEVEL control on the module front panel, that permits the video to be set according to the input level. The range of R2 is

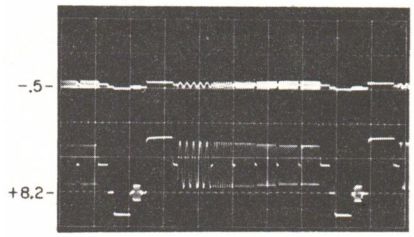




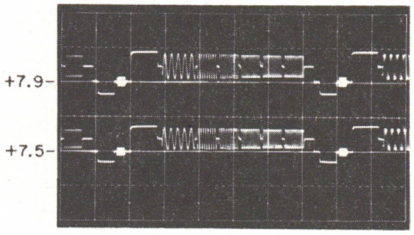
A. TP1, 402
0.2 v/cm
10 μs/cm



B. Top: Q1 emitter
Bottom: Q1 base
Both: 0.2 v/cm, 10 μs/cm



C. Top: Q5 emitter, .05 v/cm
Bottom: Q5 collector, 1 v/cm
Both: 10 μs/cm



D. Top: Q6 base
Bottom: Q6 emitter
Both: 2 v/cm, 10 μs/cm

All waveforms in E-E mode.

Figure 3—Input and Equalization, Schematic Diagram and Typical Waveforms

sufficient to supply the required signal level (approximately 0.5 volt) at the base of Q1 when the input level is between 0.5 and 2.0 volts peak-to-peak.

Video through switch S1 is connected through parasitic suppression resistor R8 to the base of emitter follower Q1. This transistor serves as an equalizer driver, and together with common base stage Q5, forms an emitter-coupled amplifier.

With switch S1 in the UNITY position as in normal operation, video current from the emitter of Q1 is simply coupled through resistors R13, R17 and R19 into the emitter of Q5. This current passes almost undiminished to the collector of Q5, then through R21, the collector load resistance, where the video current develops a corresponding video voltage.

The voltage gain obtained with this circuit is approximately equal to the ratio of the collector and emitter resistances, which is 5.5. Thus, a signal level of approximately 2.75 volts is developed across resistor R21.

Capacitor C2 with resistor R6 comprise a high frequency compensation network to boost frequencies in the region above 200 kHz by a small amount and overcome losses in the emitter circuit of Q5. Conventional shunt peaking is provided by inductor L1 to counteract capacitance across the collector of Q5.

When S1 is in the VAR position, video at the emitter of Q1 is fed through an equalizing circuit consisting of two RC branches. One branch, composed of R14 and C3 in combination with R13, causes high frequency components to be attenuated. The other branch, consisting chiefly of C4 and HF COMP potentiometer R18, causes a peaking of high frequencies, depending on the position of the HF COMP control. With the control fully counterclockwise, capacitor C4 is effectively out of the circuit and the rolloff characteristics of R14/C3 prevail.

As the HF COMP control is rotated progressively in a clockwise direction, the peaking effect of R18/C4 gradually overcomes the fixed rolloff of R14/C3, and finally at maximum clockwise position the peaking effect predominates. Thus, a variable frequency response characteristic is obtained that ranges from a rolloff of 2 dB to a peaking of 3 dB at 3.6 MHz, in order to compensate for deficiencies in the incoming signal.

When the HF COMP control is set at the center of its range, the rolloff and peaking branches are close to neutralizing each other. This results in a flat response.

Emitter follower Q6 is used to minimize loading of the high impedance output of common base amplifier Q5. The low impedance output of the emitter of Q6 helps establish isolation between the filter driver stage and the monitor circuits that this stage drives.

Video Distribution

This circuit consists of two emitter followers that couple one output of the equalizer amplifier to two series amplifier driver stages. Each driver stage, in turn, supplies two video outputs from the module. Refer to figure 4.

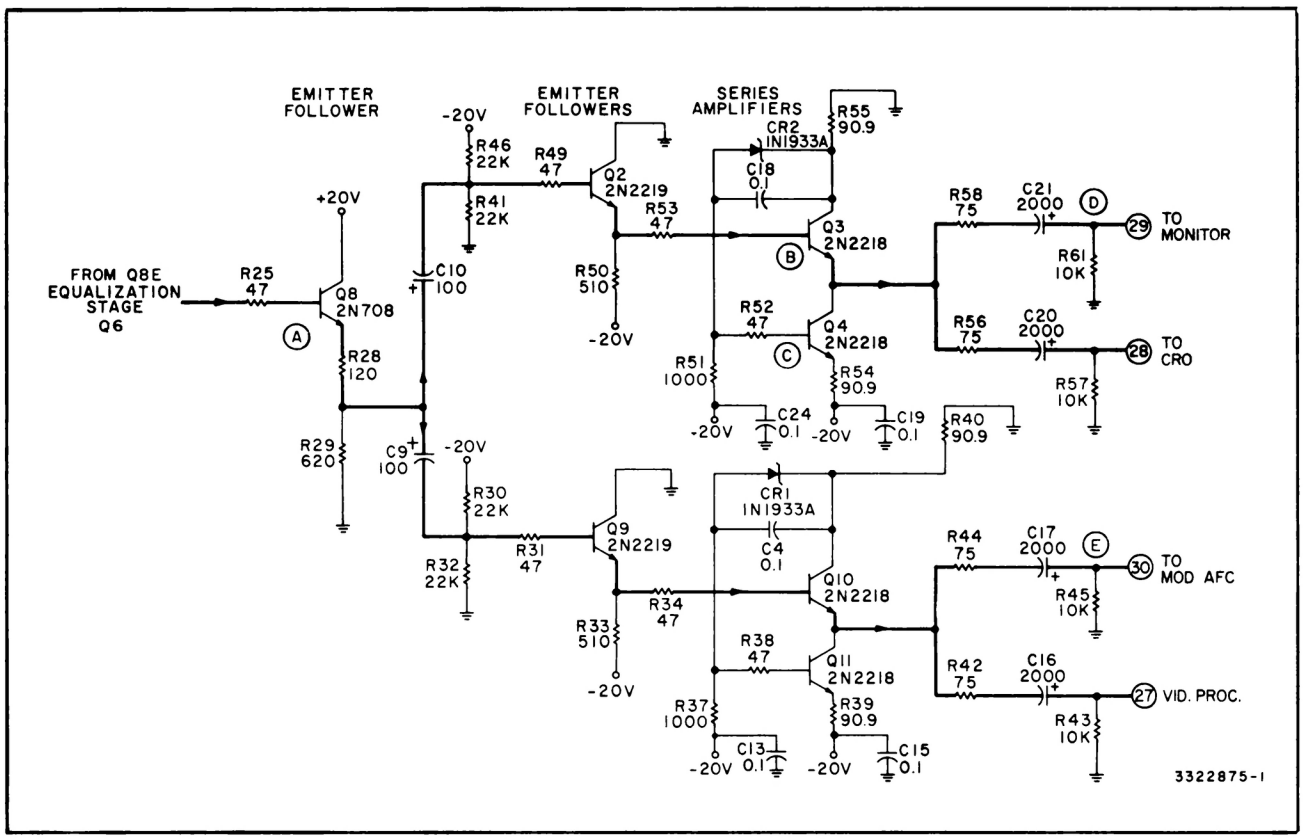
One emitter output from Q6 in the input and equalization circuit is connected through parasitic suppressor R25 to the base of Q8. The emitter output from Q8 drives a voltage divider consisting of resistor R28 and R29. This voltage divider reduces the 2.5-volt signal level at Q8 emitter to 2.0 volts required to feed the line driver stages.

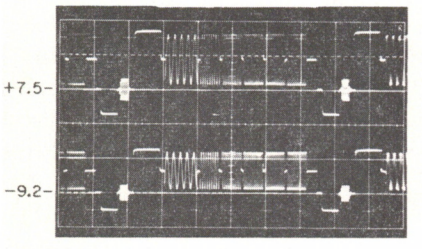
An output from the voltage divider is coupled through capacitor C10 to the base of emitter follower Q2, which functions as a driver for the series amplifier that follows. The emitter output from Q2 is connected to the base of Q3 (through resistor R53), which is the driver input.

Transistors Q3 and Q4 are cascaded to form a series amplifier. The collector output of Q3 is coupled to the base of Q4 through capacitor C18 and resistor R52. The emitter output of Q3 is combined with the collector output of Q4 since both are in phase. The output level at this junction point is two volts peak-to-peak when one volt input is supplied to the module.

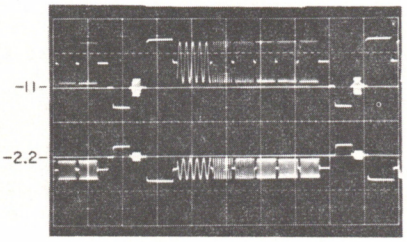
The junction of Q4 collector and Q3 emitter is the distribution point for two output signal paths from the module. One output is coupled through sending-end terminating resistor R58 and capacitor C21, leaves the module through pin 29 of P1 and is supplied to the Picture Monitor via the Monitor Switcher. The second output is coupled through R56, C20, and pin 28 and is supplied to the CRO via the CRO Switcher. Both output levels are one volt when the lines are terminated at their receiving ends.

The second output from the voltage divider is coupled through capacitor C9 to an identical circuit as that used for the monitor and CRO outputs. Transistor Q9 drives cascaded series amplifier Q10 and Q11, which form a driver to supply two additional sending-end, terminated output signal paths.

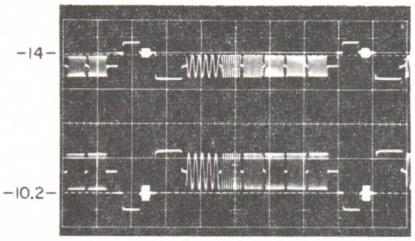




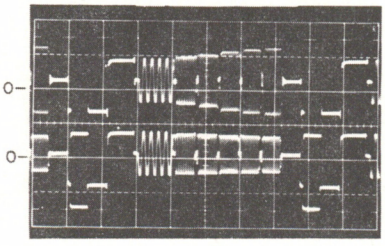
A. Top: Q8 base
Bottom: Q2 base
Both: 1 v/cm, 10 μs/cm



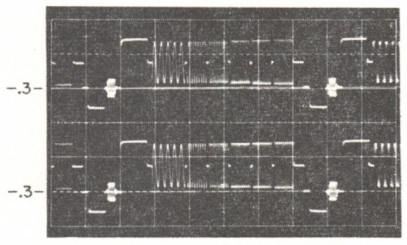
B. Top: Q3 base
Bottom: Q3 collector
Both: 1 v/cm, 10 μs/cm



C. Top: Q4 base
Bottom: Q4 collector
Both: 1 v/cm, 10 μs/cm



D. Both: Junction C21/R61
.5 v/cm, 10 μs/cm
Top: H.F. Comp. to max.
Bottom: H.F. Comp. to min.
S1 in VAR position



E. Top: Junction C17/R45
Bottom: Junction C16/R43
Both: .5 v/cm, 10 μs/cm

All waveforms in E-E mode.

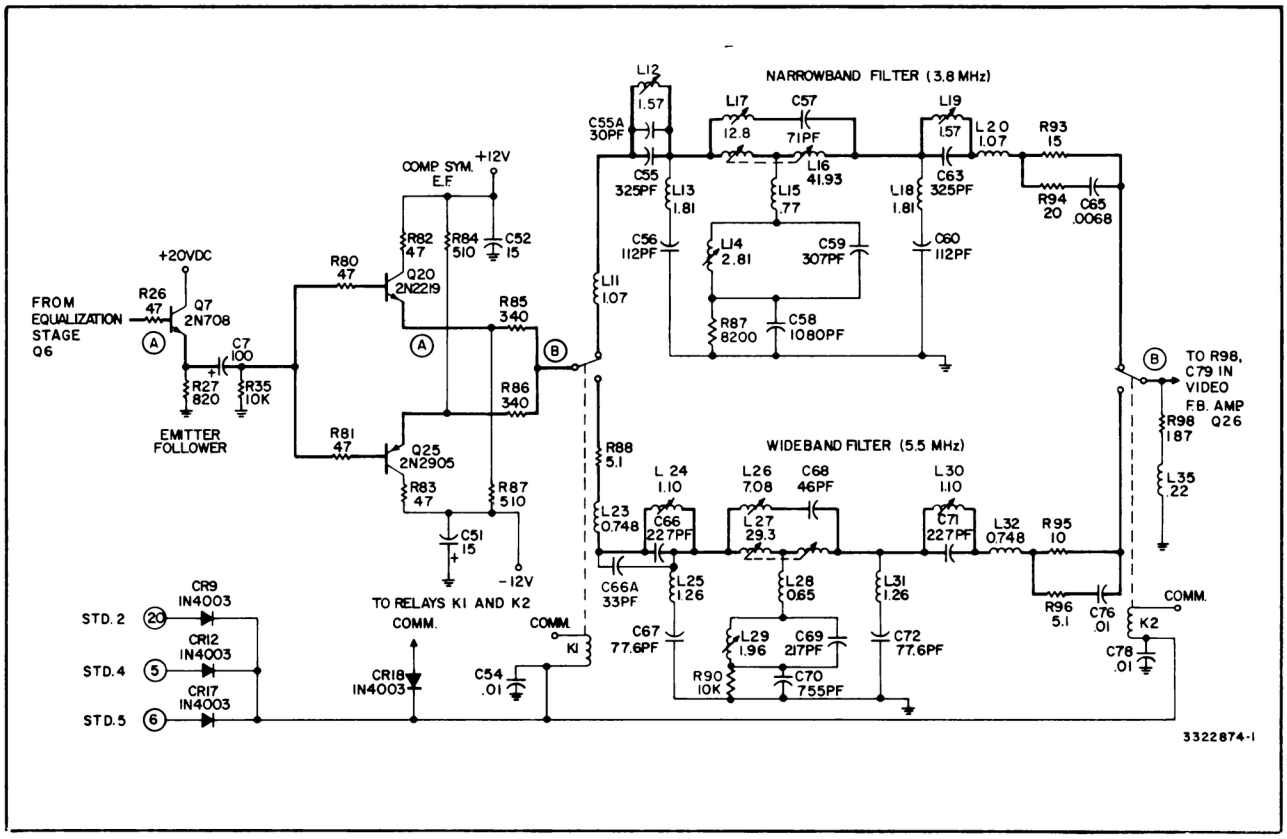
Figure 4—AFC Processor and Video Monitor Drivers, Schematic Diagram and Typical Waveforms

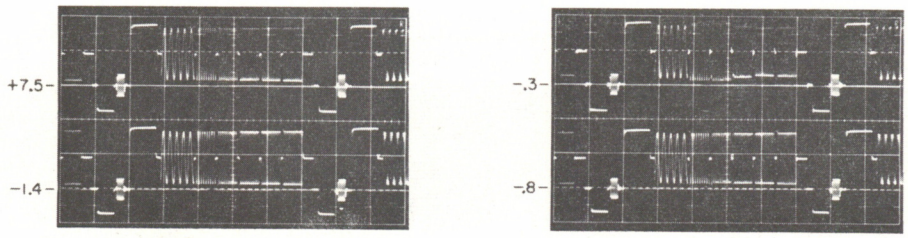
The third video output leaves the module through pin 30 and is supplied to the video input of the Modulator AFC Module, which is described later in this instruction book. The fourth output is terminated at module pin 27 and 11.

Low Pass Filters

Emitter follower Q7 provides additional isolation between the modulator and monitor channels, as well as feeding the lowpass filter driver stage. A complementary symmetry emitter follower (CSEF) is used for the driver to insure undistorted transfer of both positive- and negative-going transitions.

A CSEF stage is used to overcome undesirable reactive effects caused by the filter loading. The output of the emitter in a PNP type transistor normally provides rapid response to the negative-going portion of the signal; however, during the positive-going portion, the reactance in its emitter circuit is discharged slowly and produces a slope. In a NPN type





A. Top: Q7 base
Bottom: Q20 emitter
Both: 1 v/cm, 10 μs/cm

B. Top: K1 arm
Bottom: K2 arm
Both: .5 v/cm, 10 μs/cm

All waveforms in E-E mode.

Figure 5—Wideband and Narrowband Filters, Schematic Diagram and Typical Waveforms

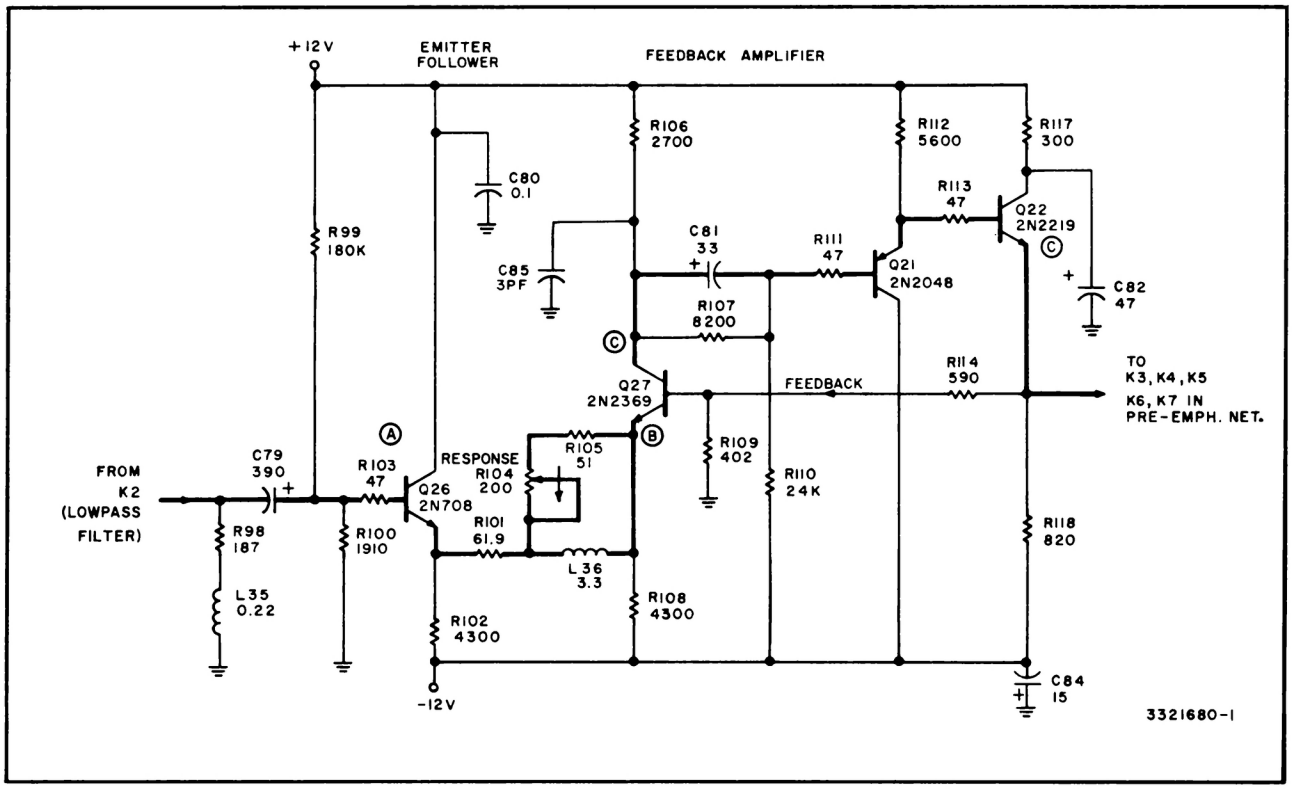
transistor, the opposite condition exists, with a rapid response to positive-going signals, but slow discharging during negative-going portions. Thus, complementing the desirable characteristics of both transistor types produces accurate reproduction of the high-frequency video signal.

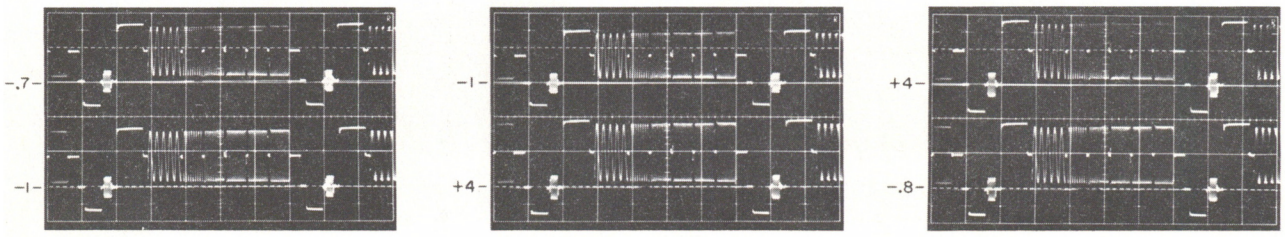
Resistors R85 and R86, driven by the low output impedance of the CSEF are essentially in parallel with each other. These feed the selected lowpass filter at its characteristic impedance of 170 ohms.

Filter selection is determined by the state of relays K1 and K2, as listed in table A1. The narrowband filter is used for 405/525 lowband monochrome and color standards. The wideband filter is used on all other standards. Refer to figure 5.

Both filters are essentially similar except for the differences in component values necessitated by cutoff frequency. The characteristics are listed in the aforementioned table. The filters are of an unbalanced configuration having been derived by a transformation from a balanced form. Elements that cannot be directly converted to the unbalanced configuration are accommodated by the bridged T section with mutual coupling. This type of mesh is located at the center of each filter.

A receiving-end termination of 170 ohms is presented to the filter by resistor R98 and inductor L35 in parallel with the input impedance of the stage that follows.





A. Top: Q26 base
Bottom: Q26 emitter
Both: .5 v/cm, 10 μs/cm

B. Top: Q27 emitter, .5 v/cm
Bottom: Q27 collector, 1 v/cm
Both: 10 μs/cm

C. Top: Q27 collector
Bottom: Q22 emitter
Both: 1 v/cm, 10 μs/cm

All waveforms in E-E mode.

Figure 6—Video Feedback Amplifier, Schematic Diagram and Typical Waveforms

Video Feedback Amplifier

Filtered video is ac-coupled through capacitor C79 to the base of Q26. This transistor is an emitter follower that couples the video to the input of the feedback amplifier. The emitter output of Q26 is supplied through resistor R101 and the resistor-inductor network using inductor L36, resistor R105 and potentiometer R104. The latter is adjusted to provide for a flat response in conjunction with the feedback amplifier. Refer to figure 6.

The emitter of Q27 is the input to the feedback amplifier using transistors Q27, Q21 and Q22. The amplified output from the collector of Q27 is coupled uninverted through capacitor C81 and parasitic suppressor R111 to the base of Q21, which supplies its emitter output to Q22. Feedback is taken from the amplifier output at the emitter of Q22 and is supplied through resistor R114 to the junction of resistor R109 and the base of Q27. The voltage gain of this amplifier is determined approximately by the relation: (R114/R109) + 1 = (509/402) + 1 = 2.46. The feedback amplifier output drives the selected pre-emphasis network which follows.

Pre-Emphasis Network

Output from the video feedback amplifier is supplied in parallel to one set of normally-open contacts in each of the relays K3 through K7. The second set of normally-open contacts in the relays is connected in parallel to the amplifier and Modulator driver circuit which follows. Refer to figure 7.

Relays K3 through K7 each have a special resistor-capacitor network connected between their two center-arm contacts. Any one of these RC networks is connected in series with the video signal path by energizing the relay associated with that network. The network thus selected is both driven and terminated by extremely low impedances created by the feedback amplifiers.

Each pre-emphasis network consists of two resistors in series, one of which is paralleled by a capacitor, as shown in the simplified schematic diagram. At low frequencies, the capacitive reactance of the network is so high that capacitor C1 is ineffective and only resistors R1 and R2 are effectively in the circuit. The value of these resistors thus determines the video level supplied to the Modulator, and thereby sets the

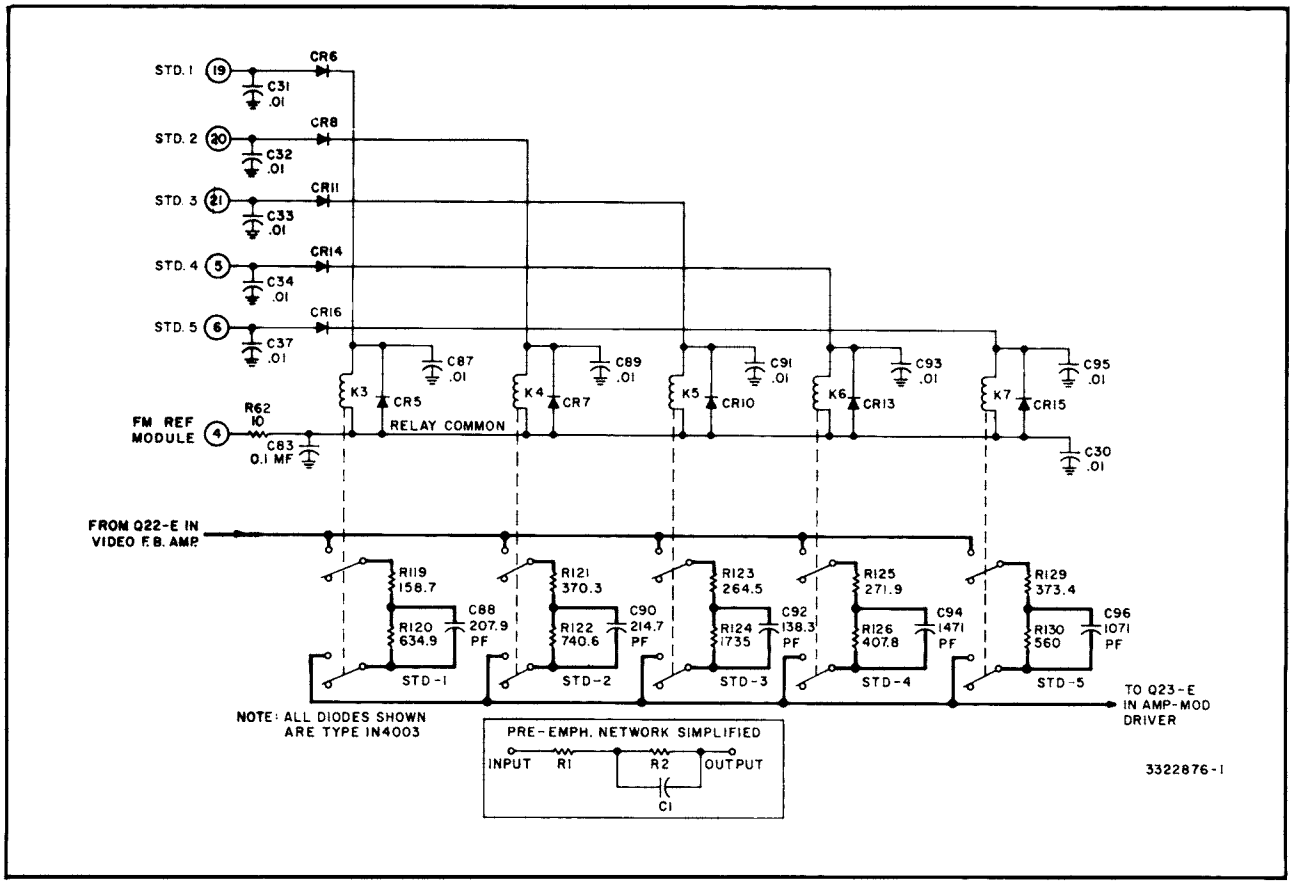


Figure 7—Pre-Emphasis Network, Schematic Diagram

low frequency FM deviation according to the standard selected. The relative Modulator drive level for the various standards is tabulated in table 2. The magnitude of resistance in the pre-emphasis networks, represented by resistors R1 and R2 in the simplified schematic diagram, is in an exact inverse relationship to these relative levels.

As the video frequency increases, the capacitor in the pre-emphasis network becomes increasingly effective in bypassing resistor R2 until, at the highest operating frequencies, the resistor is completely bypassed. Thus, at high frequencies the Modulator drive is determined by the value of the unbypassed resistor, and is considerably higher than at lower video frequencies during which time both resistors are in series. The ratio of low frequency-to-high frequency drive for each standard is listed as A_{HF}/A_{LF} in table 2, and is a measure of the degree of pre-emphasis imparted to the video modulating signal.

The video signal frequency at which pre-emphasis becomes effective (often designated as the *turnover frequency*) is determined by the value of the capacitor and the relation of its reactance to the resistance in the network.

One terminal of each pre-emphasis relay coil is connected to a single bus (relay common) which is normally energized by −26 volts. The opposite coil terminal of each relay is connected to one of five standards buses through an isolation diode to the standards selector switch.

Selection of a given operating standard connects ground to a corresponding bus through the standards generator and operates the appropriate relay. It is not desirable to allow the signal to pass through the Video Input module when in the Noise test mode, therefore the −26 volt supply to the relay common bus is disconnected when the NOISE TEST pushbutton is energized. This prevents any of the relays from being operated and allow a signal to pass.

Amplifier and Modulator Driver

Pre-emphasized video from the selected RC network is direct-coupled to the input of a feedback amplifier consisting of common base stage Q23 and common emitter stage Q24. The signal is inverted in the amplifier by Q24. Part of the amplifier output at the collector of Q24 is fed through resistor R132 to the emitter at Q23. Here it is added to the input signal, with which it is out of phase by 180 degrees. Feedback therefore tends to cancel out the input signal. Refer to figure 8.

The amplifier output level is automatically regulated so that the resultant signal at the emitter of Q23 is essentially zero. Thus the voltage gain from the input of the pre-emphasis nework to the output of the amplifier is equal to the ratio of resistor R132 to the impedance of the selected pre-emphasis network. For example: on HIGH BAND operation, the low frequency gain is R132/(R125 + R126) = 681/(271.9 + 407.8) = 1.0. At high frequencies, R126

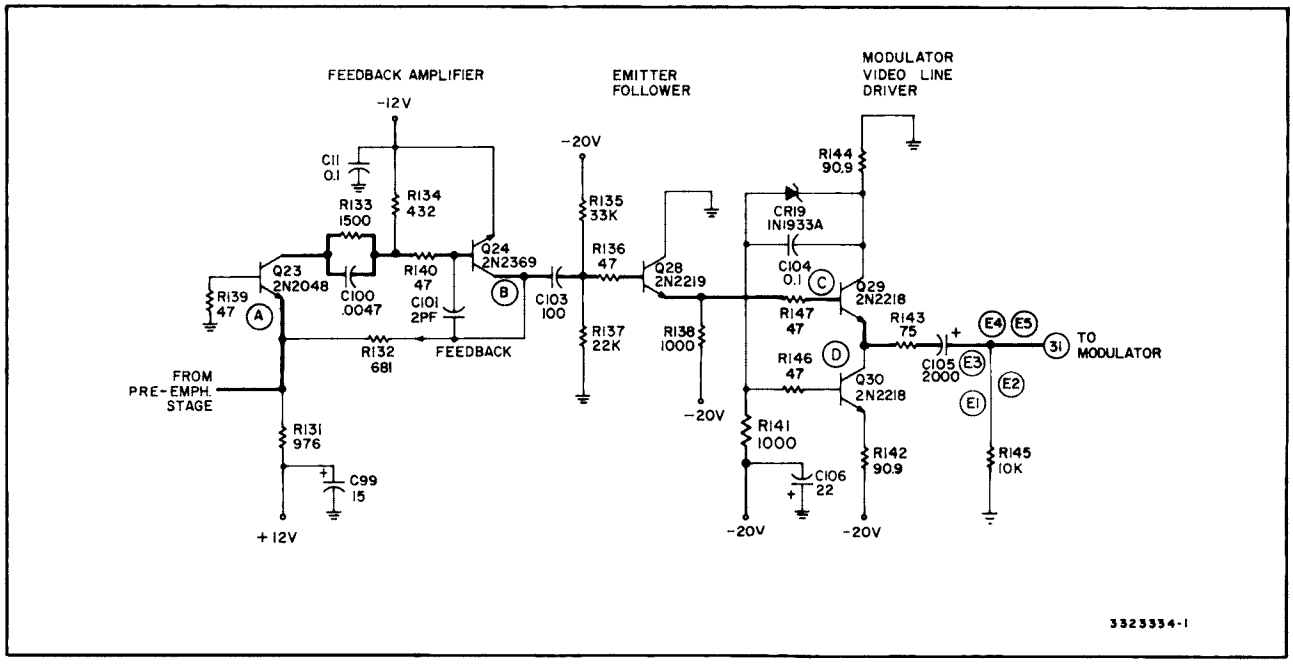
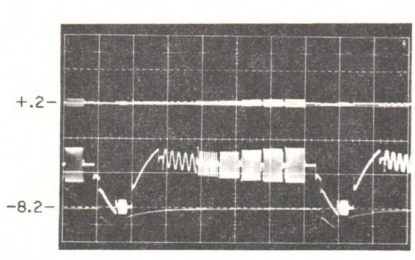
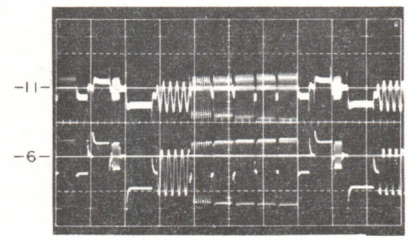


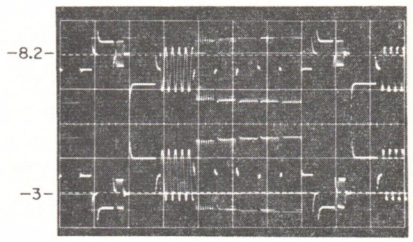
Figure 8—Amplifier and Modulator Driver, Schematic Diagram and Typical Waveforms



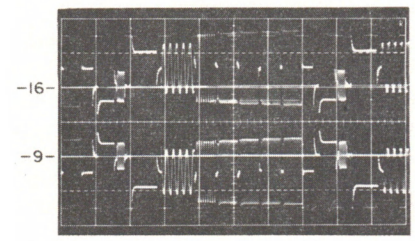
A. Top: Q23 emitter
Bottom: Q23 collector
Both: .05 v/cm, 10 μs/cm



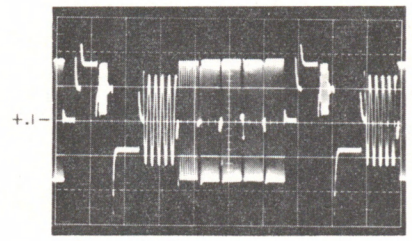
B. Top: Q24 base, .05 v/cm
Bottom: Q24 collector, 2 v/cm
Both: 10 μs/cm



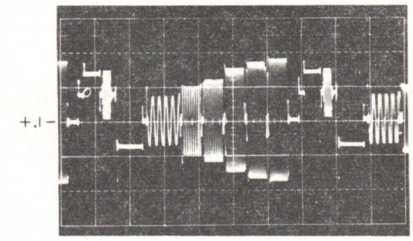
C. Top: Q29 base, 2 v/cm
Bottom: Q29 collector, .5 v/cm
Both: 10 μs/cm



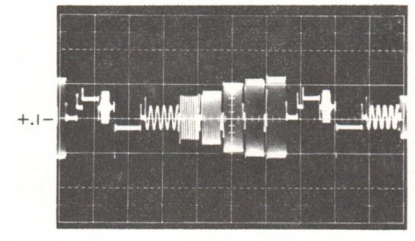
D. Top: Q30 base, .5 v/cm
Bottom: Q30 collector, 2 v/cm
Both: 10 μs/cm



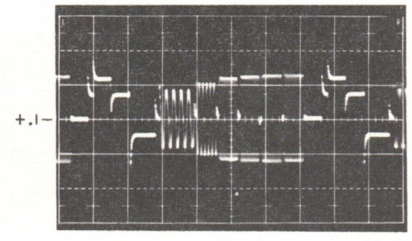
E1. P1 pin 31, .5 v/cm, 10 μs/cm
Highband Standards
525 Lines



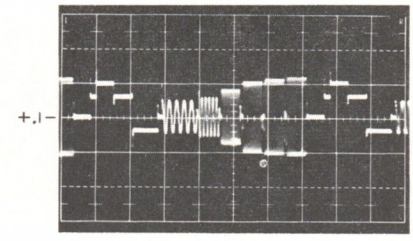
E2. P1 pin 31, .5 v/cm. 10 μs/cm
Lowband Mono Standards
525 Lines



E3. P1 pin 31, .5 v/cm, 10 μs/cm
Lowband Color Standards
525 Lines



E4. P1 pin 31, .5 v/cm, 10 μs/cm
Highband Standards
625 Lines



E5. P1 pin 31, .5 v/cm, 10 μs/cm
Lowband Mono Standards
625 Lines

All waveforms in E-E mode.

Figure 8—Amplifier and Modulator Driver, Schematic Diagram and Typical Waveforms (Continued)

is completely bypassed by C94, therefore the gain is R132/R125 = 681/271.9 = 2.5. Note that the 2.5:1.0 ratio is the A_{HF}/A_{LF} that is listed for this standard in table 2.

Resistor R134 is the collector-load resistance for Q23, and R133 permits establishing proper dc conditions in the amplifier. Capacitor C100 bypasses high frequencies around resistor R133 from the collector of Q23 to the base of Q24. Smooth response at high frequency without peaking results with feedback through capacitor C101.

The collector output of Q23 is coupled through capacitor C103 to the base of Q28. Emitter-follower Q28 direct-couples the video signal through parasitic suppressor R147 to the base input of the Modulator video line driver.

Transistors Q29 and Q30 are series amplifiers that provide video output to the Modulator module. The collector output from Q29 is coupled through capacitor C104 to the base of Q30. The collector output from Q30 is combined with the emitter output from Q29 (both are in phase with sync positive) and feed their outputs through sending-end terminating resistor R143 and coupling capacitor C105 out of the module via pin 31.

ADJUSTMENTS

The Video Input module has been carefully adjusted at the factory and should not be disturbed. Except for the Termination Trim potentiometer (R2) and the Gain Trim potentiometer (R4), all internal adjustments have been locked at their proper settings with a red or blue sealing compound. If adjustment is required on sealed controls, contact your RCA representative.

Termination Trim Adjustment

The input termination for the video input module is adjusted as follows:

1. Apply operating power to the machine.

2. Set the UNITY-VAR switch (S1) to the VAR position.

3. Note its present position, and rotate the VIDEO LEVEL control (R6) to its fully counterclockwise position.

4. Connect a resistance bridge to pin 17 of plug P1 (with no input connected to the machine at jacks 12J1 or 12J2).

5. Adjust terminating trim potentiometer R2 for an input resistance of 75 (±0.5) ohms.

6. Remove the resistance bridge and return the VIDEO LEVEL to its original setting.

Gain Trim Adjustment

The gain trim potentiometer (R4) is adjusted as follows:

1. Connect the signal generator output to the video input of the module at pin 17 of plug P1 or on VIDEO test point TP1. Set the signal generator to supply an output of one kHz at 1.0 volt peak-to-peak.

2. Calibrate the preamplifier on the oscilloscope input (with the input probes) to obtain identical gain on both channels while the oscilloscope vertical gain is set at 0.02 volt-per-centimeter.

3. Connect one oscilloscope input probe to VIDEO test point TP1 and the other input probe to the module video processor output on pin 27 of P1.

4. Set the UNITY-VAR switch (S1) to the UNITY position. Apply power to the machine.

5. Adjust gain trim potentiometer R4 on the module to obtain an identical output level indication on both inputs of the oscilloscope.

NOTE: Do not disturb the above setting of R4 for the remainder of the adjustments to the module.

6. Move the vertical input probe that is presently connected to pin 27 of P1 and connect it to the outputs for the modulator afc on pin 30, CRO on pin 28, and monitor on pin 29. The level indication for each of these pins should be without plus or minus two percent of the level indication obtained for test point TP1.

MODULATOR MODULE

CIRCUIT DESCRIPTION

General

The Modulator module is used during RECORD and E-E modes of operation to provide an FM carrier that is modulated according to the pre-emphasized video signal supplied from the Video Input module. If the video signal were to progress through the record and playback signal paths in its normal form, severe limitations would normally be encountered due to the non-linearity and limited frequency spectrum imposed by the magnetic characteristics of the record/playback heads and the tape. However, with a constant amplitude signal that is frequency modulated according to the amplitude fluctuations of the video signal (such as is supplied by the Modulator module) the limitations are effectively overcome.

In normal operation, relay K2 in the Modulator module remains deenergized and video is used for frequency modulation through the module. Refer to figure 9. Video input is supplied through the DEVIATION control on the module front panel for adjustment of the video drive level to the frequency modulators (described later). The signal then passes through the normally-closed contacts of relay K1 to the complementary emitter followers Q1 and Q2. The relative outputs from these two emitter followers are adjusted with an internal Video Balance control, then coupled through emitter followers Q3 and Q4 to respective clamp drivers.

Each clamp driver feeds a separate clamping capacitor in associated high and low frequency channels. Video in each channel is clamped during the back porch interval to a reference voltage potential that is dependent on the following:

1. A dc level from the FM Reference module.

2. The position of the VERNIER FREQ control on the Modulator module front panel.

3. A fixed bias level obtained from a Zener diode and resistor networks.

4. The AFC error pulse amplitude and its polarity.

Balanced clamp pulses are supplied from the Modulator AFC module, and are coupled through capacitors associated with separate clamp circuits. Clamped video then passes through the normally-closed contacts of relay K2, and separate low-pass filters to varactors CR17 and CR18. The varactors (voltage

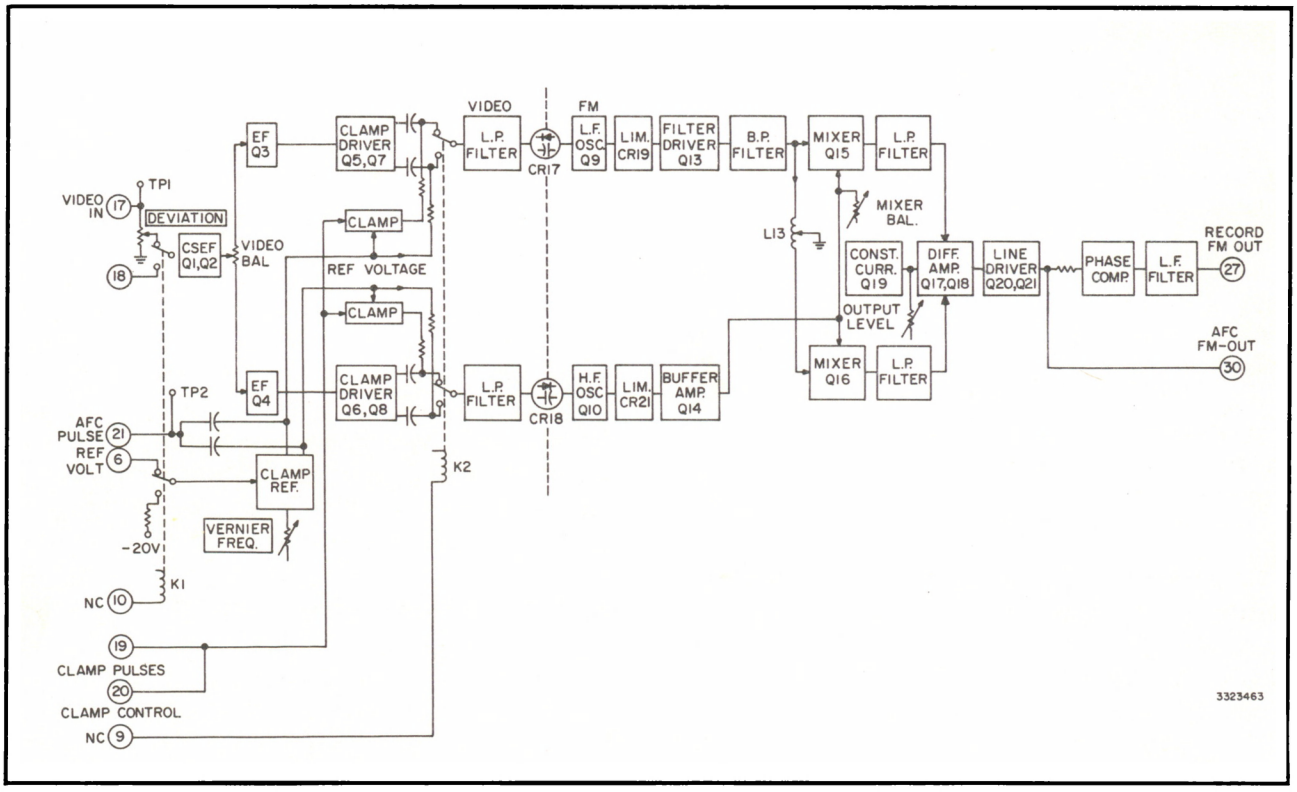


Figure 9—Modulator Module, Block Diagram

TABLE 3—MODULATION FREQUENCIES

FUNCTION	*STANDARD (Freq. in MHz)*				
	1 *525* *LB Mono*	*2* *625* *LB Mono*	*3* *525* *LB Color*	*4* *525* *Highband*	*5* *625* *Highband*
Sync Tip	4.28	4.95	5.5	7.06	7.16
Blanking	5.0	5.4	5.79	7.9	7.8
Peak White	6.8	6.8	6.5	10.0	9.3
H.F. Osc.—Gray	107.25	107.25	107.25	108.75	108.5
L.F. Osc.—Gray	101.25	101.25	101.25	99.75	100.0
Gray	6.0	6.0	6.0	9.0	8.5

variable diode capacitors) are used to control the frequency of the low frequency and high frequency oscillators, Q9 and Q10 respectively, according to variations of the instantaneous voltage level present in the video.

Polarity of the video signal, the clamp reference voltage, and the varactors is such that as the video amplitude changes toward sync level, it increases the frequency of the low frequency oscillator while simultaneously decreasing the frequency of the high frequency oscillator. Typical oscillator frequencies for each operating standard are listed in table 3.

Lowpass filters are used between the clamps and the oscillators to prevent rf from feeding back into the video circuits. The filters also provide part of the reactance required for the oscillator tuned circuits that follow the varactors.

Each oscillator output is limited through respective high and low frequency limiters to remove amplitude modulation that would cause spurious frequency components in the Modulator output. The low frequency limiter output is amplified through Q13 and filtered through a filter having a bandpass of 90 to 110 MHz to remove all undesired components from the low frequency channel. The high frequency limiter output is supplied to buffer amplifier Q14.

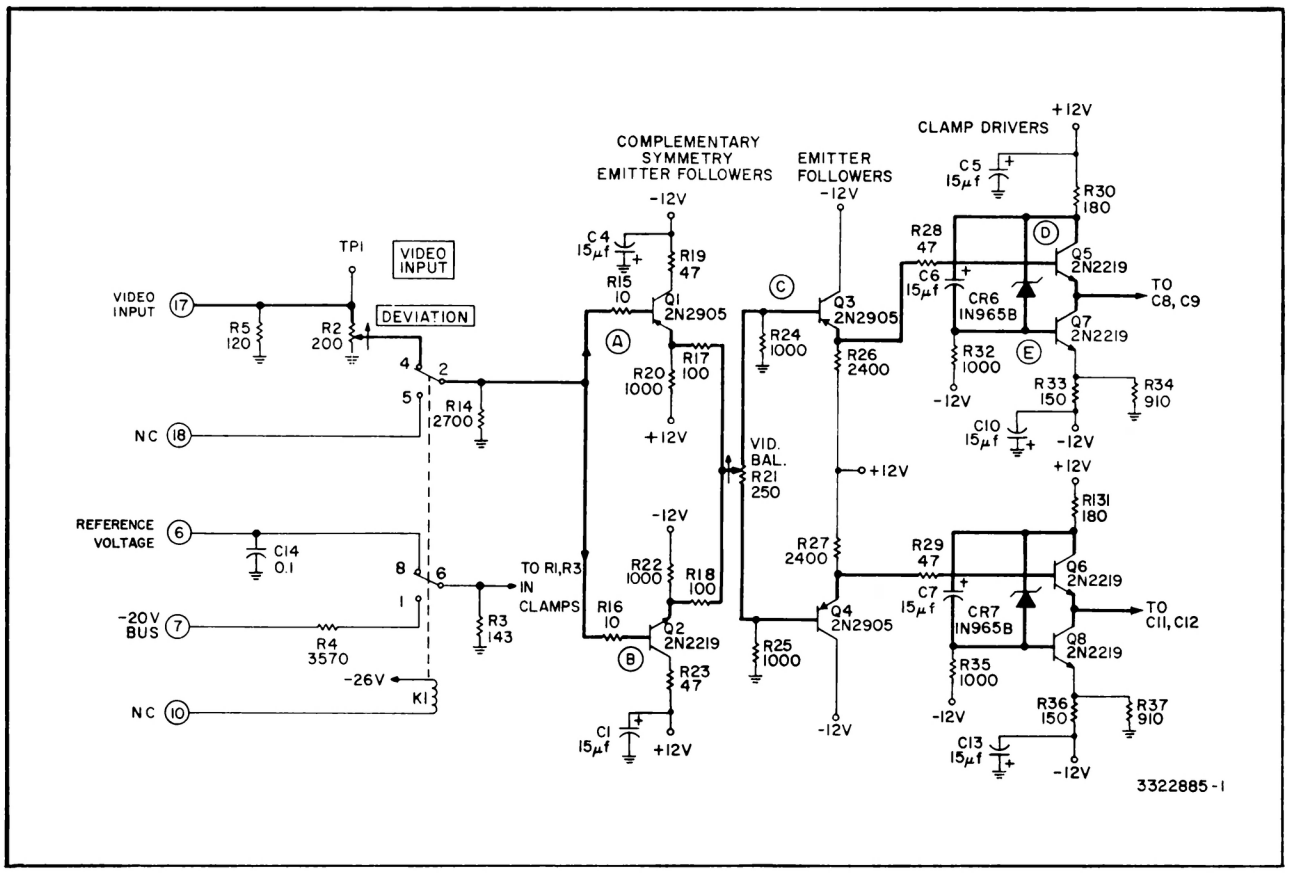
Output from the bandpass filter in the low frequency channel drives mixer Q15/Q16 in push-pull by means of autotransformer L13. The high frequency channel output from buffer amplifier Q14 drives the mixer in an unbalanced manner. Eventually, the high frequency signal is cancelled out by the common mode rejection of the differential amplifier that follows; however, the low frequency channel components are not cancelled. A Mixer Balance potentiometer is included to permit accurate balancing of the mixer, thereby avoiding generation of spurious frequencies in the mixer.

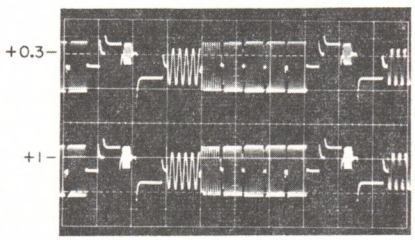
Outputs from mixer Q15/Q16 are supplied through separate lowpass filters having linear phase shift characteristics. The filters reject oscillator frequency products above 30 MHz but pass the difference frequencies that form the desired FM signal spectrum. Filtered push-pull fm is then supplied to differential amplifier Q17/Q18 which functions with constant current source Q19. An Output Level potentiometer is included between amplifier Q17 and Q18 to control the level of the single-ended output from Q18.

A single output is supplied from differential amplifier Q17/Q18 to fm line drivers Q20 and Q21, which in turn, supply two outputs. One output from the line drivers leaves the module as the AFC fm output to the Modulator AFC module to provide for AFC when that mode is selected. The second line driver output is coupled through a phase compensation network that compensates for phase shift characteristics of the bandpass filter in the low frequency oscillator channel. The phase-compensated signal is fed to the Record Switch module through a lowpass filter to remove residual high frequency products that have not been cancelled in the mixer.

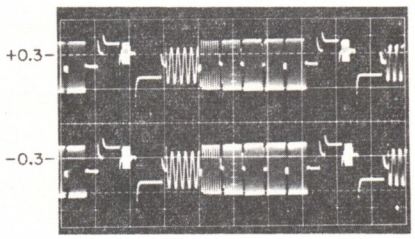
Input Balance and Clamp Drivers

Pre-emphasized video is supplied from the Video Input module to the Modulator module via pin 17 of plug P1, and is terminated at 75 ohms with resistor R5 and potentiometer R2. Test point TP1 is provided to check the video signal prior to the frequency-modulation process. Refer to figure 10.

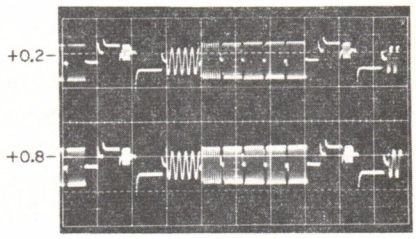




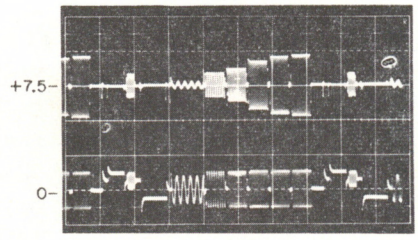
A. Top: Q1 base
Bottom: Q1 emitter
Both: 1 v/cm, 10 µs/cm



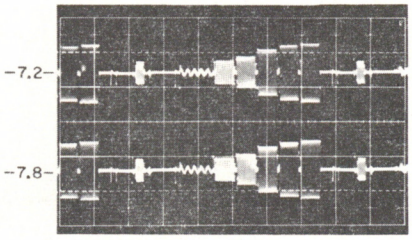
B. Top: Q2 base
Bottom: Q2 emitter
Both: 1 v/cm, 10 µs/cm



C. Top: Q3 base
Bottom: Q3 emitter
Both: 1 v/cm, 10 µs/cm



D. Top: Q5 collector, .2 v/cm
Bottom: Q5 emitter, 1 v/cm
Both: 10 µs/cm



E. Top: Q7 base
Bottom: Q7 emitter
Both: .2 v/cm, 10 µs/cm

All waveforms in E-E mode.

Figure 10—Input Balance and Clamp Drivers, Schematic Diagram and Typical Waveforms

The signal amplitude at the input of the module (after termination) depends on the sync tip to peak white deviation required by the standard selected for operation. Relative levels required for each standard are listed in table 3.

Video is supplied through DEVIATION potentiometer R2, which is adjusted so that video signal variations result in the correct amount of carrier swing (deviation) for the chosen standard. It should be noted that *relative* levels between standards are determined by the Video Input module, but the *absolute* level on any standard is set by the DEVIATION control. Once set for any standard, the control need not be readjusted when a different standard is selected.

From the DEVIATION control, video passes through the normally-closed contacts of relay K1 and proceeds to the junction of parasitic suppression resistors R15 and R16 in the base inputs of Q1 and Q2. Another set of contacts on relay K1 transfers a dc voltage to the clamp reference input. This reference voltage originates in the FM Reference module and is fed to K1 through pin 6 of P1.

Video is coupled through emitter followers Q1 and Q2 and through mixing resistors R17 and R18. The junction of these resistors drives Video Balance potentiometer R21, located on the module chassis.

The Video Balance potentiometer is set to obtain optimum cancellation of non-linearity in the oscillator stages in the module. This is accomplished by setting the signal level on the bases of Q3 and Q4 with the voltage divider network using resistors R24, R25 and potentiometer R21. Moving the potentiometer in either direction from center position increases the video level to one transistor base while simultaneously decreasing the level to its counterpart base. This optimizes Modulator linearity by compensating for differences in oscillator deviation sensitivity.

Emitter followers Q3 and Q4 begin the two separate channels (high and low frequency) that are used in the Modulator module. Each emitter follower couples the balanced video to succeeding clamp drivers, which in turn apply video to the clamps.

The clamp drivers for both channels are identical series amplifiers that provide single-ended push-pull performance. Their design serves to cancel out nonlinearity of the individual transistors and supply the signal at a very low output impedance. Because they are identical, only one is described.

Resistors R33 and R34 control the current through transistors Q5 and Q7. This is determined by the bias setting on the base of Q7 with Zener diode CR6. The collector output from Q5 is coupled through CR6 (for lower frequencies) and capacitor C6 (for mid and higher frequencies) to the base of Q7. The collector output of Q7 is in phase with the emitter output of Q5 and therefore provides current amplification to drive the clamp capacitor that follows, as well as to provide low impedance for the succeeding low-pass filter.

The entire circuit to this point presents no gain to the video signal. Gain through the series amplifier is unity; however, losses incurred in previous circuits of the module present an overall gain (loss) of approximately 0.8.

Signal amplitude from sync tip to the peak white level determines the peak-to-peak deviation of the incoming signal. Thus the DEVIATION control on the Modulator front panel is effectively a sensitivity control for the module.

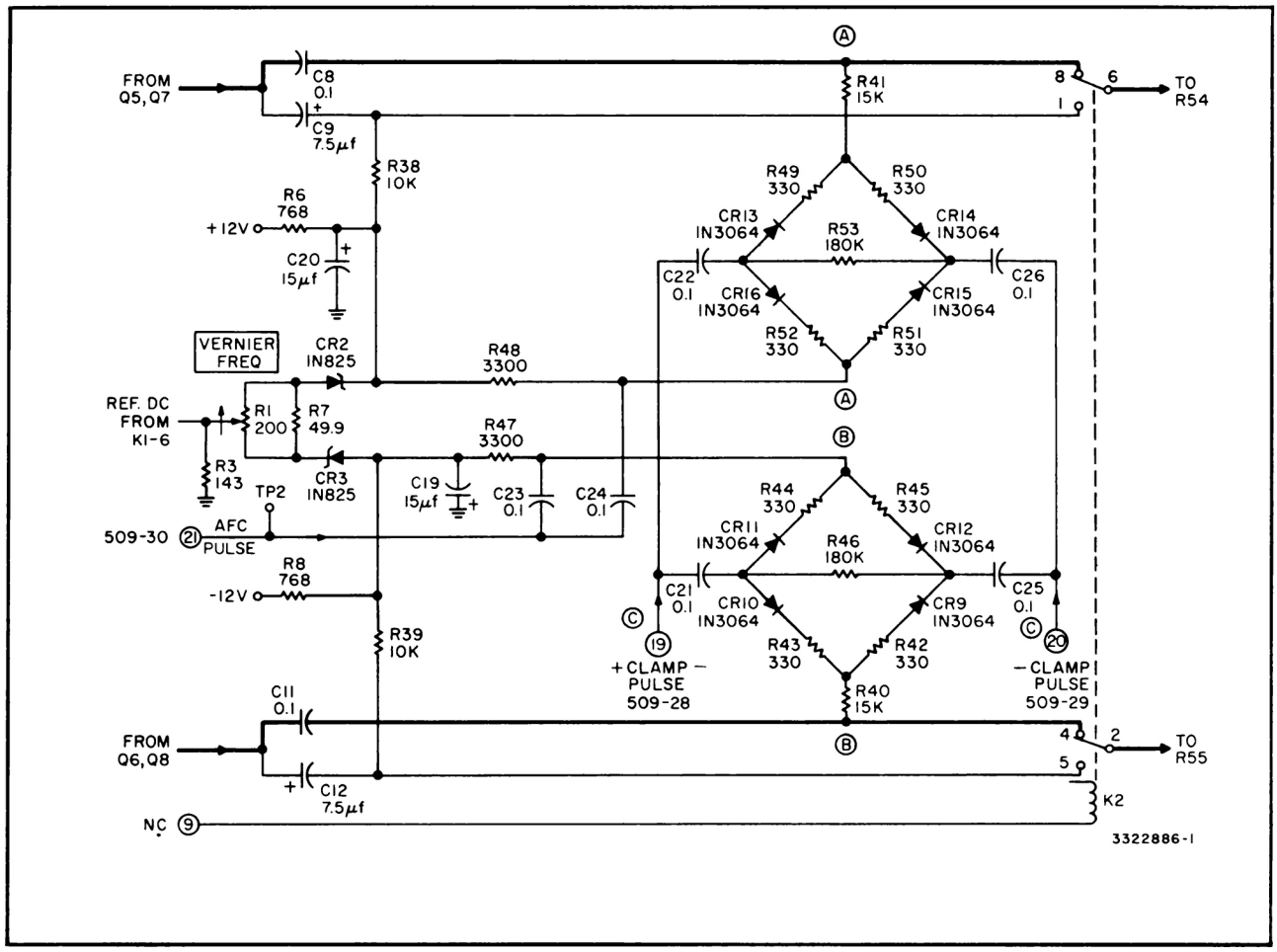
Clamps

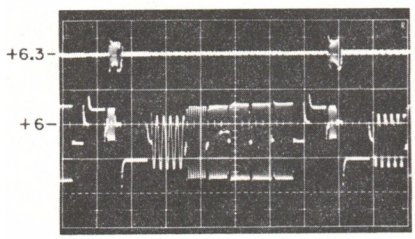
Basically the clamps are two identical diode bridges that operate as switches which close during the back porch interval. They are identical, except for the polarity of the dc reference to which they clamp. With this understanding, only one clamp bridge is described. Refer to figure 11.

Operation of the clamps is determined by the mode selected. Either the normal operating or the test mode.

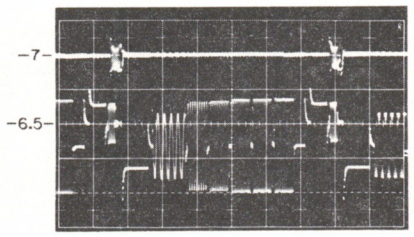
During normal operation relays K1 and K2 remain deenergized. Under this condition, the ac video signal amplitude variations supplied from clamp driver Q5/Q7 is placed at a dc potential with respect to ground according to the reference voltage supplied from the FM Reference module via relay K1-6, and the instantaneous dc level present on the AFC error signal supplied by the Modulator AFC module via pin 21 of P1.

Each time the back porch occurs, clamp pulses having equal but opposite polarity are applied in parallel through coupling capacitors to each bridge. A positive pulse supplied via pin 19 and a negative pulse through pin 20 are coupled through capacitors C22 and C26, respectively, to cause the bridge to close and allow the reference voltage to pass from the junction of R51/R52 to the junction of R49/R50. This dc reference then places a dc component on video that is coupled through capacitor C8.

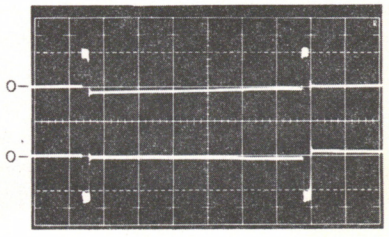




A. **Top: Junction R48/C24, 2 v/cm**
Bottom: R41/C8, .5 v/cm
Both: 10 μs/cm



B. **Top: Junction R47/C23, 2 v/cm**
Bottom: Junction R40/C11, .5 v/cm
Both: 10 μs/cm



C. **Top: P1 pin 19**
Bottom: P1 pin 20
Both: 5 v/cm, 10 μs/cm

All waveforms in E-E mode.

Figure 11—Clamp Circuits, Schematic Diagram and Typical Waveforms

Reference dc supplied through pin 2 on the contacts of relay K1 is applied to the center arm of VERNIER FREQ potentiometer R1, through the potentiometer and to Zener diode CR2. During normal operation, the VERNIER FREQ control presents no change in operating frequency of the module due to the AFC function.

Due to the biasing arrangement on Zener diode CR2, the reference voltage places the cathode of CR2 more positive with respect to its anode. Breakdown voltage through the diode is 6.2 volts, which inserts a fixed bias for proper voltage range of operation of the varactor in the low-frequency oscillator. The reference dc voltage is then decoupled with RC network R48 and C20 to prevent the AFC error bus from being loaded by the reference supply source.

Once decoupled, the dc reference voltage becomes modified to a higher or lower potential according to

the AFC error (if any). The AFC error is supplied from the Modulator AFC module in the form of negative or positive pulses which are added algebraically to the reference dc voltage. This presents a corrective influence on the dc component of the video as it is supplied to the varactors in the event that the back porch (blanking) frequency from the Modulator is incorrect. If the Modulator frequency is too high AFC error pulses during back porch will be positive and *add* to the decoupled reference dc.

Reference dc with corrective AFC error added (when a frequency error exists) is now applied to the input of the bridge at the junction of resistors R51/R52. Each time the back porch occurs, clamp pulses coupled through capacitors C22 and C26 cause the bridge to close and allow the corrected reference dc to pass to the video line via the junction of resistors R49/R50. Thus, the back porch establishes the frequency point at which the carrier is to operate, and therefore affects the Modulator frequency of all other brightness relationships in the video signal.

Limitation on the rate at which the AFC can correct the carrier frequency is imposed by the time constant of the RC network using R41 and C8. Resistor R41 also serves to prevent the clamp reference circuit from shorting video bus during clamping.

Video is now supplied with a dc component through the normally-closed contacts of relay K2, in two channels, to resistors R54 and R55 in the filter inputs of the voltage controlled oscillators and limiter stage.

Voltage Controlled Oscillators and Limiters

The two video channels, which have been modified by the reference dc, are supplied through the contacts of relay K2. Video clamped to the reference dc is supplied through the normally-closed contacts. One video channel feeds low-frequency oscillator varactor CR17 through sending-end terminating resistor R54 and the lowpass filter consisting of C29, L1, C30. The opposite video channel feeds varactor CR18 to control the high-frequency oscillator. Refer to figure 12.

The high frequency channel lowpass filter has an added section to present a delay to that video channel and compensate for the fixed delay in the bandpass filter that follows the low-frequency oscillator. This permits modulation on both oscillators to arrive at the mixer with no timing deviations.

Video frequency response is not affected by the presence of the filters because their cutoff frequencies are above 15 MHz. Thus they permit video components to pass unimpeded to the varactors but prevent

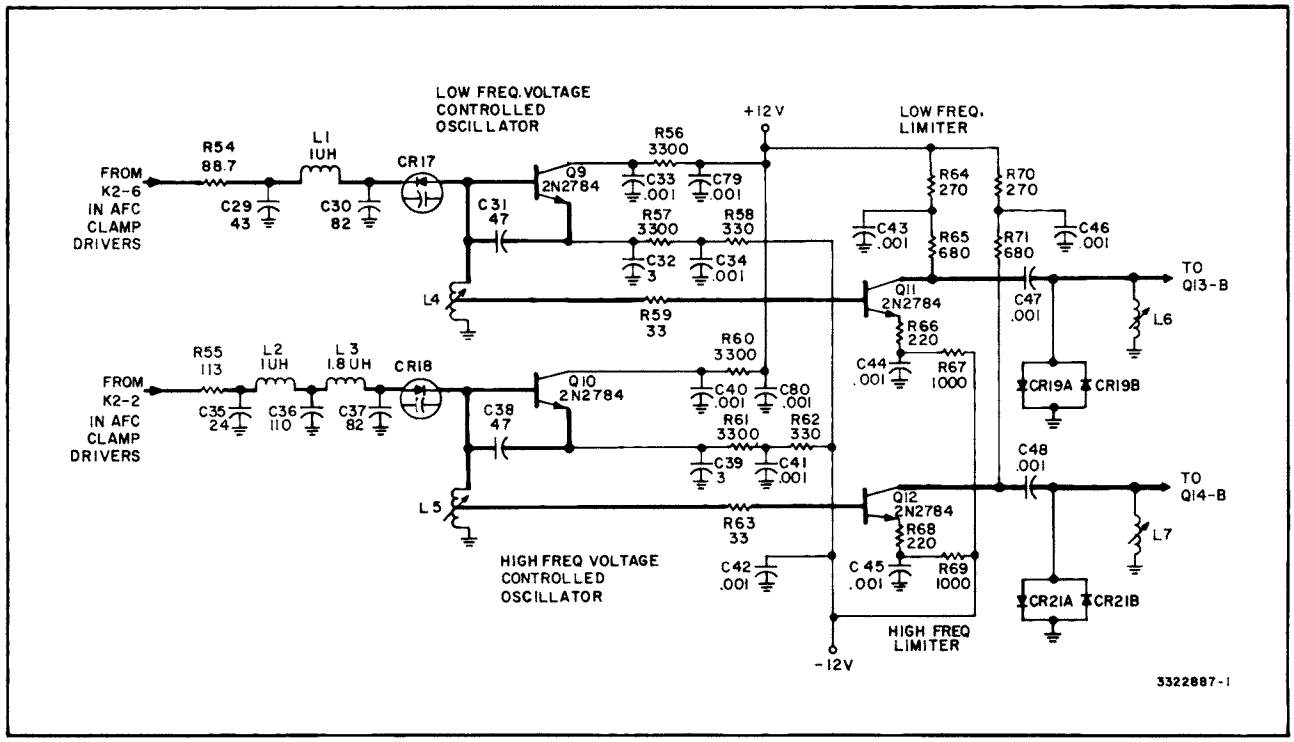


Figure 12—Voltage Controlled Oscillators and Limiters, Schematic Diagram

reverse flow of high-frequency oscillator components above their pass band, back into the video circuits.

The low-frequency and high-frequency oscillator circuits are essentially identical, therefore only the low-frequency oscillator is described. Transistor Q9 is employed in a Colpitts circuit with its collector held at ac-ground with capacitor C33. The oscillator tuned circuit consists of tapped inductor L4, varactor CR17, and the total reactance presented at the output terminal of the lowpass filter.

Capacitors C31 and C32 control the level of feedback in the oscillator by forming a capacitive voltage divider across the tank circuit for an emitter tap. The higher capacitance of C31 presents a low feedback level with respect to base drive, thereby providing maximum stability and low harmonic distortion.

Output from the oscillators is taken at low impedance from the tap of inductor L4. Current limiting resistor R57 and collector voltage dropping resistor R56 feed dc operating voltages to the oscillator.

The anode of varactor CR17 is held at dc ground potential by its connection to ground through inductor L4. The capacitance presented at the input/output terminals of CR17 depends on the bias across the varactor diode. Two bias components are presented by the Modulator. One is the steady positive dc reference voltage to which the varactor is clamped. The polarity of this reference reverse biases the varactor and causes it to operate in a high Q condition.

The second bias component of the varactor is the video signal amplitude variations. As the video signal goes positive (toward sync tip), the reverse bias on the varactor increases, thus reducing its capacity and causing the oscillator frequency to increase. When the video signal goes negative (toward white), the varactor capacitance increases and the oscillator frequency decreases. Thus, the oscillator frequency tends to follow video level variations.

A condition exists in the high-frequency oscillator that is opposite to that in the low-frequency oscillator. In this condition, varactor CR18 has its *cathode* connected to dc ground potential, and a *negative* reverse bias accompanies the video signal. Thus, as video becomes more positive (toward sync tip level), the total reverse bias decreases and results in an increase in capacity from CR18, and therefore provides a lower oscillator frequency. The high-frequency oscillator frequency therefore changes inversely to the low frequency oscillator in following video signal fluctuations.

With the conditions of the varactors, the oscillator frequencies are thus driven in opposite direction by the video signal. Both frequencies tend to converge as the level goes toward sync, and they diverge at levels representing whiter picture areas. The difference between the oscillator frequencies ultimately extracted in the mixer stage therefore is minimum at sync tip level and maximum while peak white level exists.

Each oscillator output frequency does not vary linearly with video because of the non-linear capacity-voltage transfer characteristics of varactors, and the non-linear capacity-frequency relationship of the resonant circuits. However, because the two varactors are driven in equal, but opposite directions as a result of the reversed varactor polarities, non-linearity is effectively cancelled out during the mixing (subtraction) process.

Changing from one operating standard to another results in the steady dc reference voltage being shifted by relays in the FM Reference module. This change alone would shift the entire FM spectrum up or down as required, but would not affect the peak-to-peak deviation. The latter is changed by switching the appropriate RC attenuator networks in the Video Input module.

Outputs from the low- and high-frequency oscillators is amplified by transistors Q11 and Q12, respectively. Each amplifier has a gain of three, and together with back-to-back diode pairs CR19 and CR21, form limiters to clip the oscillator signal. Clipping is required to remove amplitude modulation prior to the mixing process to avoid generation of spurious frequency components in the mixer. Variable inductors L6 and L7 resonate with stray capacitance in the center of the low-and-high-frequency oscillators range.

Bandpass Filter and Mixer

Limited fm from matched limiter diodes CR19A and CR19B is supplied to the base of filter driver amplifier Q13. A potential of approximately minus 0.6 volt is developed across silicon diode CR23 which is forward biased by its connection to minus 12 volts through resistor R83. The dc developed across diode CR23 is coupled through rf choke L10 to emitter resistors R80 and R81 to bias transistors Q15 and Q16 toward conduction. Additional bias is furnished by a resistor network which includes Mixer Balance potentiometer R86. Refer to figure 13.

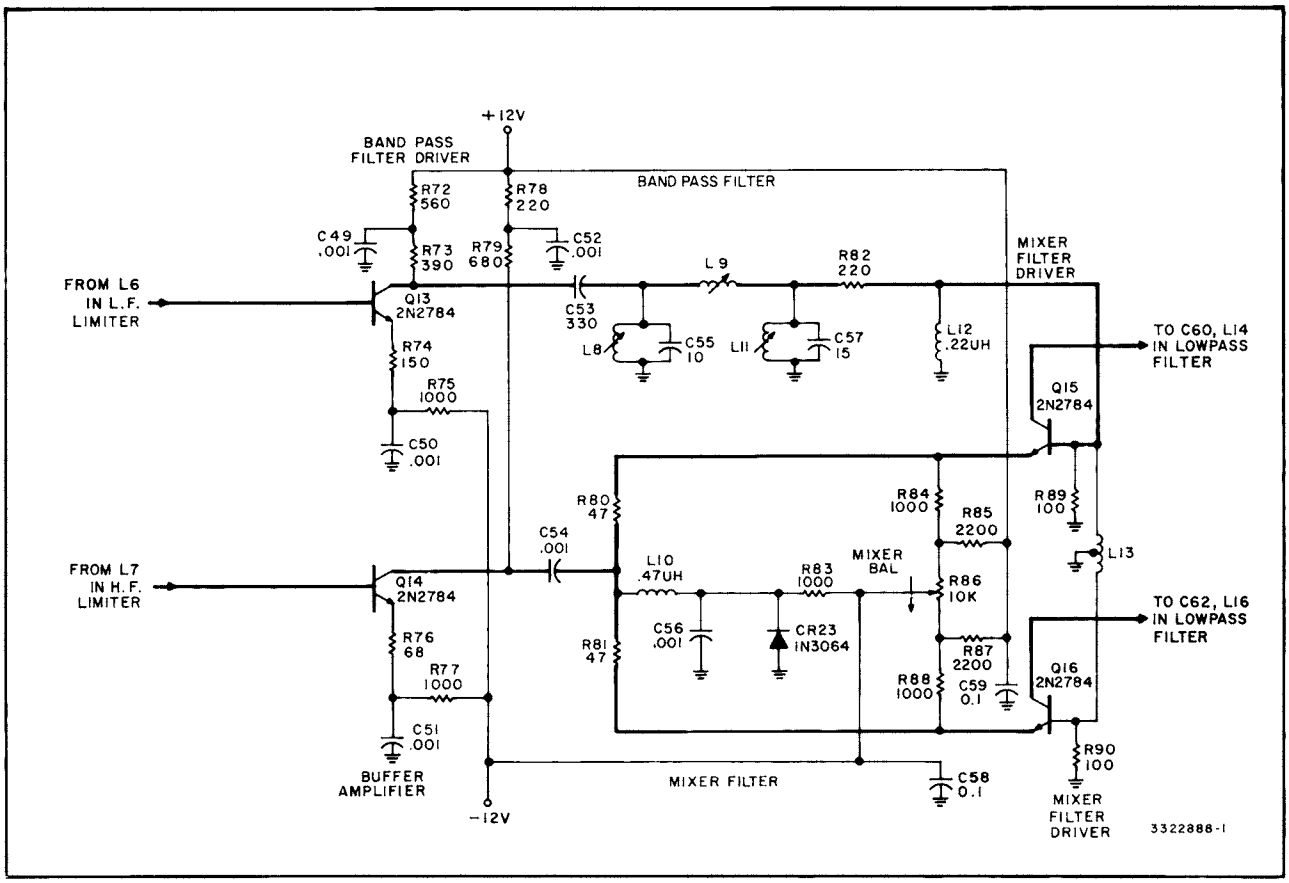


Figure 13—Bandpass Filter and Mixer Circuits, Schematic Diagram

Limited FM from matched limiter diodes CR19A and CR19B is supplied to the base of filter driver amplifier Q13. Amplified FM output from the collector of Q13 is ac-coupled through capacitor C53 to the input of a bandpass filter using inductors L8, L9, and L11, and capacitors C55 and C57. Inductor L9 functions as a mutual inductance to furnish coupling between double-tuned circuits C55/L8 and C57/L11. Tuned circuit C55/L8 determines the high frequency skirt, C57/L11 determines the low frequency skirt, and L9 influences the flat top of the bandpass. The bandpass filter provides a response that is flat to within plus or minus one percent in the operating range 90 to 110 MHz. Inductor L12 resonates the base of Q15 at 100 MHz to eliminate the effects of stray capacitance. Resistors R82, R89 and R90, in addition to terminating the filter, also substantially reduce the input signal level at the bases of Q15 and Q16.

The bandpass filter removes all the harmonics of 100 MHz and provides a pure sinusoidal voltage. This voltage is applied to inductor L13, which functions as an autotransformer having windings that are tightly coupled and with its center tap connected to ground. The ends of inductor L13 are connected to the base inputs of the mixer using transistors Q15 and Q16, to provide for push-pull input.

Limited fm output from the collector of buffer amplifier Q14 is ac-coupled through capacitor C54 to the junction of resistors R80/R81 and inductor L10. The signal is then distributed to the emitters of Q15 and Q16 to be mixed with the push-pull input applied to their bases from inductor L13.

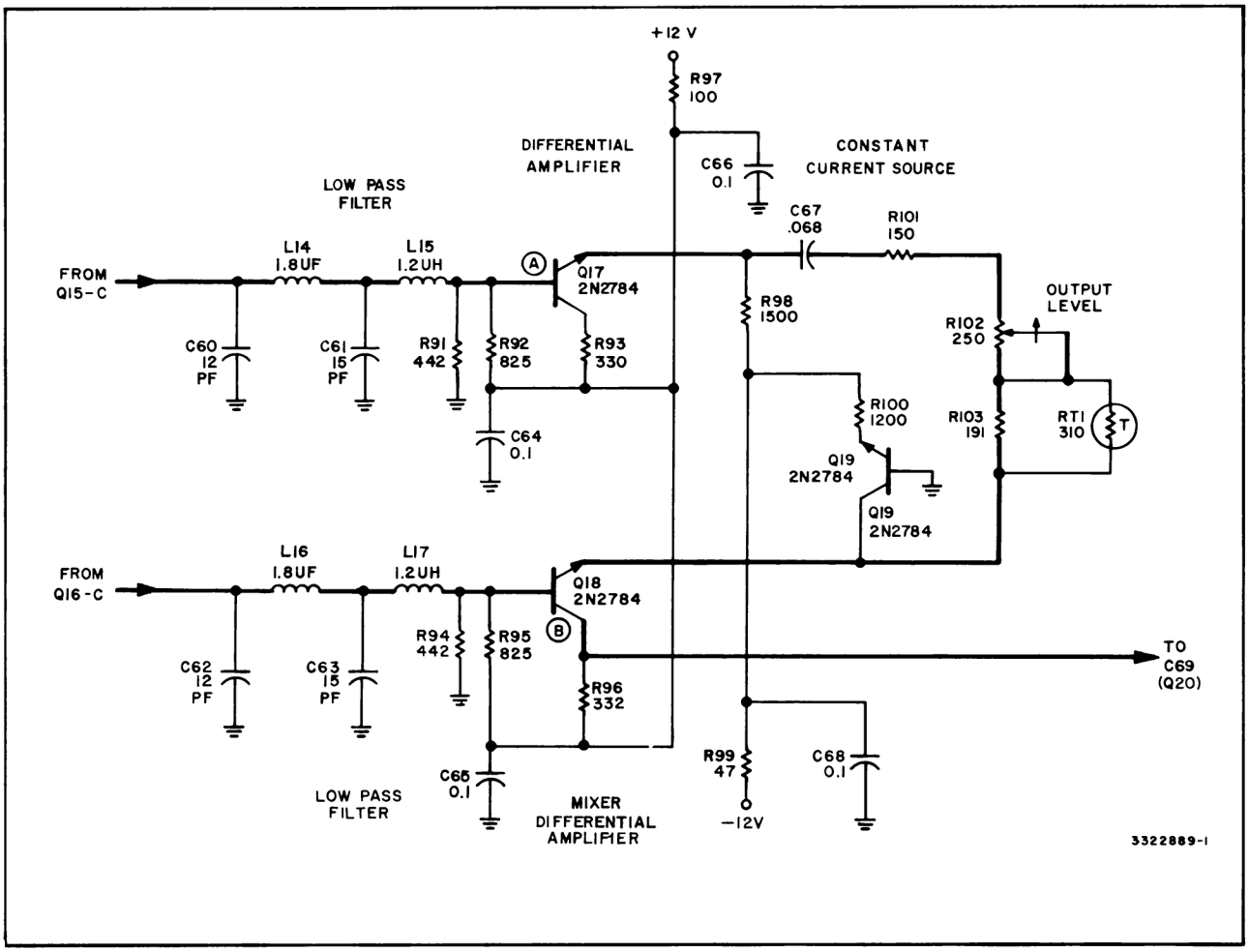
Amplitude of the fm signal driving the emitter resistors (R80/R81) is sufficient to switch transistors Q15 and Q16 on and off at the high-frequency oscillator fm carrier rate. Thus, the reduced amplitude low-frequency oscillator signal at the bases of Q15 and Q16 appears amplified at their collectors and chopped by the high-frequency oscillator signal. Since the base signal had very low distortion as a result of the bandpass filter, the desired best frequency at the mixer collector is also low in distortion. Distortion is further minimized by adjusting the bias on Q15 and Q16 emitters with the Mixer Balance control for symmetrical switching.

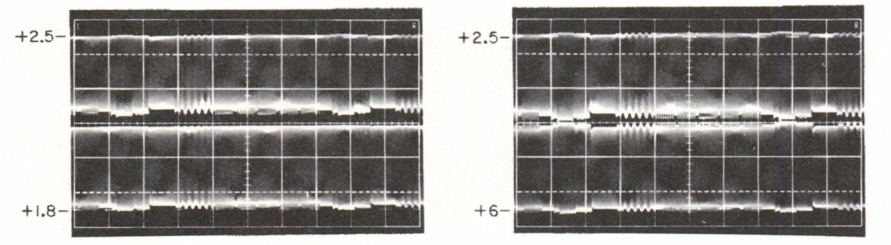
Low Pass Filters and Differential Amplifier

Frequency-modulated sine waves from the push-pull output of the mixer are supplied to two lowpass filters; one for each output of the mixer. The collector output from Q15 is supplied to the lowpass filter consisting of inductors L14 and L15, and capacitors C60 and C61. The collector output from Q16 is supplied to the filter using L16, L17, C62 and C63. Refer to figure 14.

The filters are identical and have a linear phase shift characteristic and extremely flat frequency response in the frequency range of one to 15 MHz. Their cut-off frequency is approximately 30 MHz in order to attenuate oscillator components and all products of the mixing process other than the desired difference frequencies.

The push-pull outputs from the low pass filters are supplied to the base inputs of differential ampli-





A. Top: Q17 base
Bottom: Q17 emitter
Both: .1 v/cm, 10 μs/cm

B. Top: Q18 base, .1 v/cm
Bottom: Q18 collector, .2 v/cm
Both: 10 μs/cm

All waveforms in E-E mode.

Figure 14—Low Pass Filters and Differential Amplifier, Schematic Diagram and Typical Waveforms

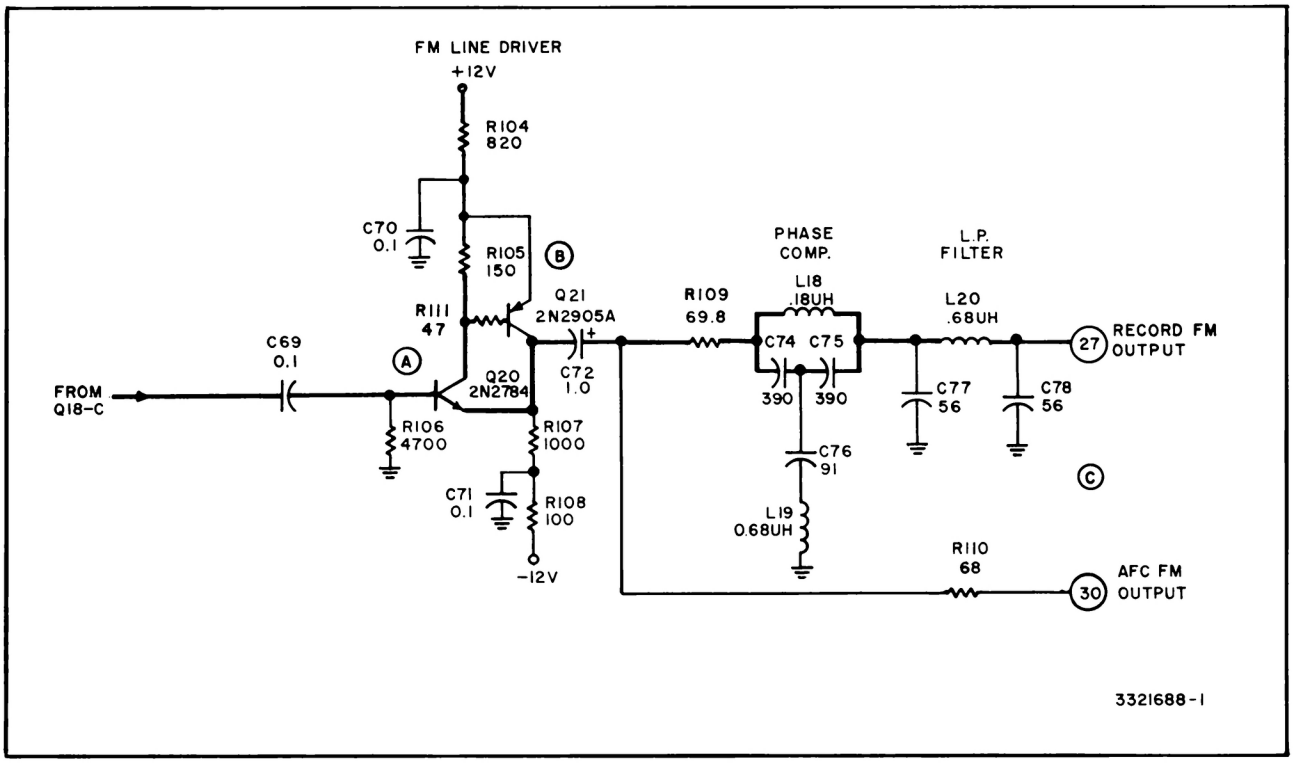
fier Q17 and Q18. DC current for Q17 is supplied through resistor R98. Transistor Q19 provides a constant dc current source for the emitter of Q18 while maintaining a high impedance to ground for the emitter.

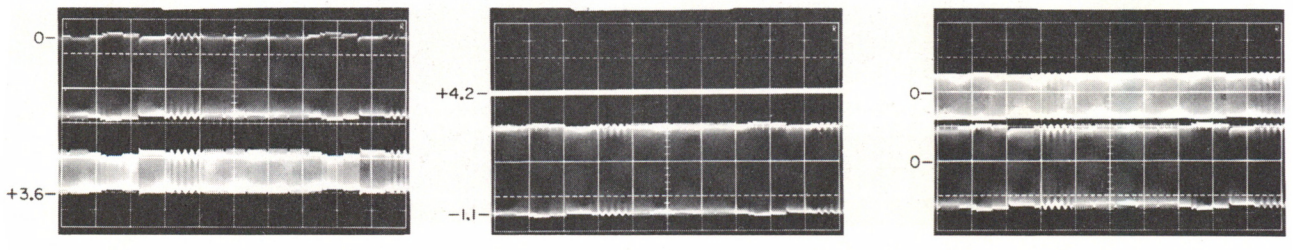
Potentiometer R102 is used to set the output level of the differential amplifier by varying the ac-coupling between the emitters of Q17 and Q18. Thermistor RT1, in parallel with resistor R103 provides for temperature compensation at the output of the differential amplifier. Capacitor C67 ac-couples the emitter of Q17 to the emitter of Q18. The two push-pull filter outputs are combined in the differential amplifier to produce a single-ended output from the collector of Q18.

Modulator Outputs

The single-ended output from the collector of Q18 in the differential amplifier is ac-coupled through capacitor C69 to the base input of Q20 in the fm line driver. Transistors Q20 and Q21 are cascaded to form a complementary feedback amplifier with unity gain. The combined output from the emitter of Q20 and the collector of Q21 (both are in phase) is ac-coupled through capacitor C72 to two signal paths. Refer to figure 15.

One output signal path is through terminating resistor R68 and pin 30 of plug P1. This signal is supplied to the Modulator AFC module for comparison with the reference frequency.





A. Top: Q20 base, .2 v/cm
Bottom: Q20 collector, .05 v/cm
Both: 10 μs/cm

B. Top: Q21 emitter, .1 v/cm
Bottom: Q21 collector, .2 v/cm
Both: 10 μs/cm

C. Top: P1 pin 27
Bottom: P1 pin 30
Both: .2 v/cm, 10 μs/cm

All waveforms in E-E mode.

Figure 15—Modulator Outputs, Schematic Diagram and Typical Waveforms

The main signal path is coupled through coupling capacitor C73 and terminating resistor R109 to the input of a phase-linearizing network. This is an all-pass network consisting of inductors L18 and L19, and capacitors C74, C75 and C76. The latter network compensates for detrimental phase characteristics which were introduced in the bandpass filter at the output of transistor Q13. The phase linearizing network feeds a 40-MHz lowpass filter consisting of capacitors C77 and C78, with inductor L20. This filter is required to completely eliminate low-frequency oscillator components which are not cancelled by the mixing process. The FM signal in the deviation range corresponding to the selected operating standard finally leaves the module via pin 27 of P1 and is supplied to the Record Switch module as the record FM signal.

Noise Test Operation

This test mode is identical to normal operation except that a fixed dc is supplied to obtain gray frequencies. AFC pulses are supplied and relay K2 remains deenergized which causes the Modulator to supply a steady carrier corresponding to gray according to the operating standard selected.

In this condition, no video is supplied because it was interrupted in the Video Input module. This allows the fixed gray carrier to be recorded so that an evaluation may be made on signal-to-noise performance of the machine.

ADJUSTMENTS

The Modulator module has been carefully adjusted at the factory and should not be disturbed. Due to the critical nature of all internal adjustments on this module, except the output level potentiometer (R102), the settings have been locked in place with a red or blue sealing compound. If service is required on any adjustment other than potentiometer R102, contact your RCA Service representative.

Output Level Adjustment

The Output Level control (R102) of the Modulator module is adjusted as follows:

1. Set the machine to operate on STD 5 (625 HB), and for normal operation with AFC pulses supplied from the Modulated AFC module. Remove the Video Input module from its slot.

2. Connect a signal generator to the VIDEO INPUT test point (TP1) on the Modulator module front panel. Set the signal generator to supply 1.0 MHz at 1.0 volt peak-to-peak.

3. Connect the oscilloscope input probe to the Record FM output of the module on pin 27 of P1.

4. Adjust the Output Level control (R102) to obtain a level indication of 0.25 volts peak-to-peak and leave it in this position.

MODULATOR AFC MODULE

CIRCUIT DESCRIPTION

General

The Modulator AFC module provides three basic functions which are described separately. Refer to the block diagram, figure 16. These are:

1. *Sync Separator.* Provides separated sync pulses derived from the input video information to establish a timing reference for the servo-systems in the machine, and also used for Modulator module clamp pulse timing and sample switch timing in this module.

This function receives its input through the normally-closed contacts of relay K3 which is permanently deenergized (not used at this time). The input is derived from the Video Input module and is amplified through transistors Q31 and Q32. The video signal is then coupled through emitter-follower Q33 to a dc restorer using a capacitor and diode network.

The dc restorer network clamps the sync tip to approximately ground potential prior to supplying the video to the differential amplifier and clipper (Q34, Q35). Input to the latter circuit is composite video and sync, whereas its output is sync only.

The differential amplifier and clipper stage provides two outputs. One is to the clamp pulse generator circuit (described later) with positive pulses, and the second output is to emitter follower Q41. The latter couples separated negative sync to complementary symmetry emitter follower Q39/Q40 which drives the transmission line with sync to the Reference Generator module.

2. *Clamp Pulse Generator.* Provides positive and negative clamping pulses for driving quad diodes in the Modulator module.

Input to this function is supplied to amplifier Q36

from transistors Q34, Q35 (described above). The positive sync pulse is amplified and inverted through Q36 to trigger the 0.8-horizontal period multivibrator (Q42/Q43/Q44). This is a monostable multivibrator whose output pulse width is determined according to the selected operating standard by the HN control supplied to it. (For any standard, the output remains at 0.8 of the horizontal period.) Its pulse width is such that it removes the one-half horizontal (0.5H) timing pulses during the vertical interval. (The horizontal period is one complete cycle of the horizontal sweep information.)

A negative 0.8-H pulse from the multivibrator is coupled through emitter follower Q45 to the three-microsecond multivibrator (Q46/Q47). This is also a monostable type and the leading edge of the 0.8-H multivibrator triggers the three-microsecond multivibrator.

Output from the three-microsecond multivibrator excites a ringing circuit which develops a partial positive half-sine wave that is coupled through emitter follower Q37. The partial sine wave causes driver Q38 to produce a square wave 1.75 microseconds long that is delayed from the leading edge of the three-microsecond pulse. The 1.75-microsecond pulse is transformer-coupled to two destinations. One winding of the transformer supplies positive and negative clamp pulses for use in the Modulator module. These pulses occur during the back porch interval. A second winding of the transformer supplies output to the AFC indicator circuit in this module.

3. *AFC.* Provides automatic frequency control (AFC) for the Modulator module based on FM signals from that module and on the black reference frequency signal obtained from the FM Reference module.

This function receives an FM input from the Modulator module and a blanking reference frequency input from the FM Reference module. The two inputs are supplied to emitter followers Q20 and Q10, respectively, which isolate these incoming signals from the sampling switch that follows. Emitter follower Q19 provides additional isolation to the FM input signal.

In the sampling switch, the positive-going sample pulse supplied from switch driver Q48 causes fm to pass through the transformer during sample pulse time, and blanking references to pass at all other times.

FM during sample pulse time and blanking reference are supplied from the sampling switch to a group of limiters. These limiters (Q4 through Q9) clip the FM and reference signals (which may originally be of unequal amplitudes) to be limited to a single, even amplitude for frequency demodulation through Q17 and Q18.

Transistors Q17 and Q18 form a frequency demodulator circuit which detects the difference in frequency between the blanking reference frequency and the FM signal. Because FM is sampled during the back porch, its frequency should equal the black or blanking reference input signal. If these two signals are of equal frequency at the AFC demodulator, no error is detected and therefore, no output is supplied from the detector. However, if a frequency error exists between the incoming FM and blanking reference, the demodulator converts this error to an amplitude variation and feeds it through the succeeding low-pass filter.

The error pulse polarity is determined by the direction of frequency error, and its amplitude is determined by the degree of error (e.g. a positive pulse results when the blanking frequency is higher than the reference frequency). (Typical AFC pulse conditions are shown in figure 18.) Low level error pulses from the low-pass filter are amplified through feedback amplifier Q2/Q3 and supplied through a second low-pass filter. The error pulse is then coupled through emitter follower Q1 and supplied to two paths.

In one path the signal is fed to a diode clipper, then through the closed contacts of relay K2 to the Modulator module where frequency correction takes place in the FM carrier. The clipping circuit on the output line prevents error pulse amplitudes that might cause improper operation of the Modulator. The second path of the error signal is supplied to an error detecting diode bridge. This bridge is clamped "on" during the back porch interval to allow error pulses to pass through a filter which maintains the peak error amplitude between pulses. The constant error level is then fed to switching transistors Q14 and Q16. A combiner stage that follows (Q13/Q14) combines the outputs of the switches to provide a common dc level to amplifier Q11/Q12.

If the error pulse is of sufficient amplitude to reach a threshold point of either switch, one transistor in the switch saturates. This condition is transferred through the combiner to amplifier Q11/Q12 which saturates, thus illuminating the MOD FREQ warning indicator.

An E-E switch that is completely independent of all other functions and circuits in the module is in-

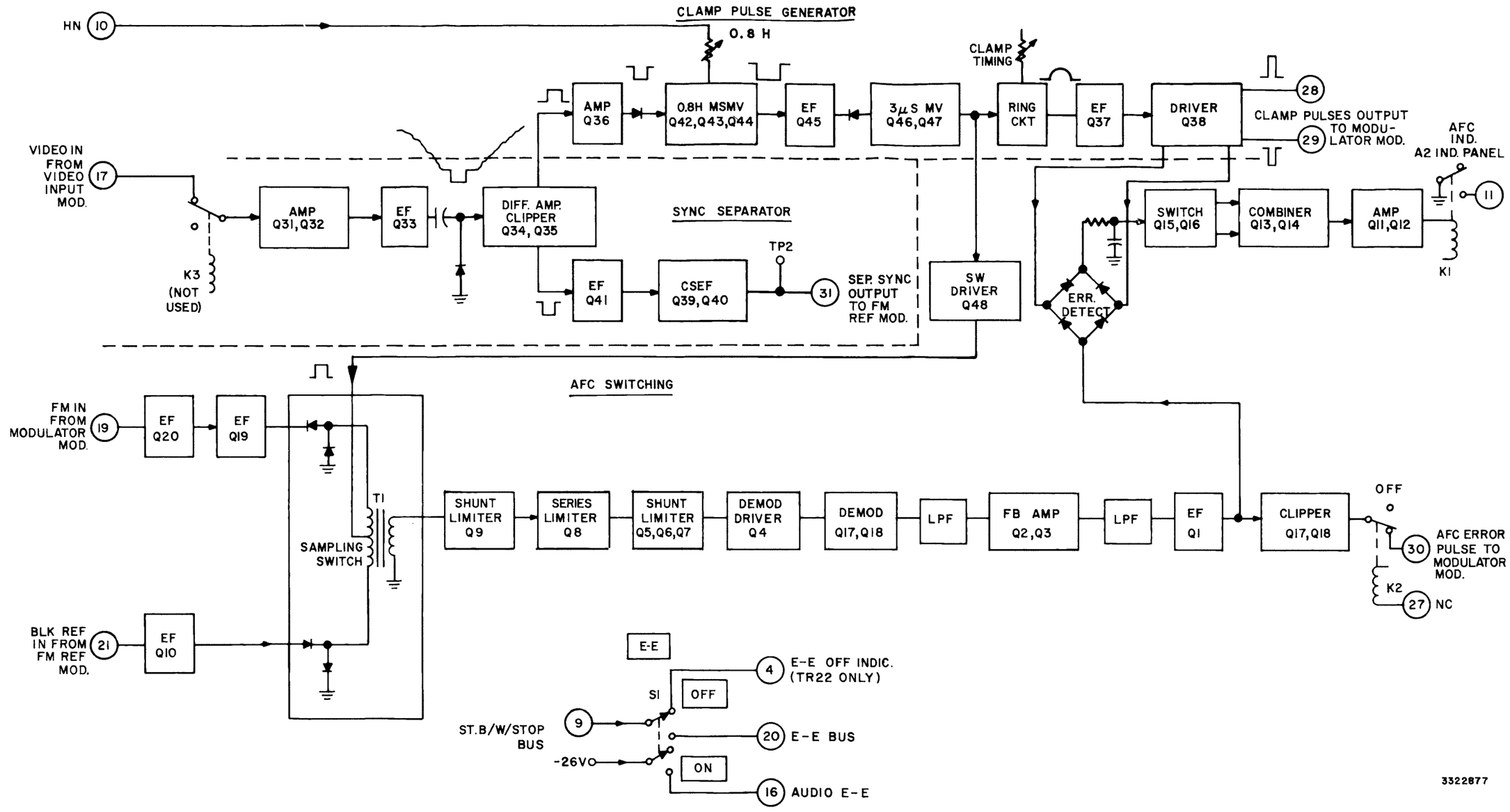


Figure 16—Modulator AFC Module, Block Diagram

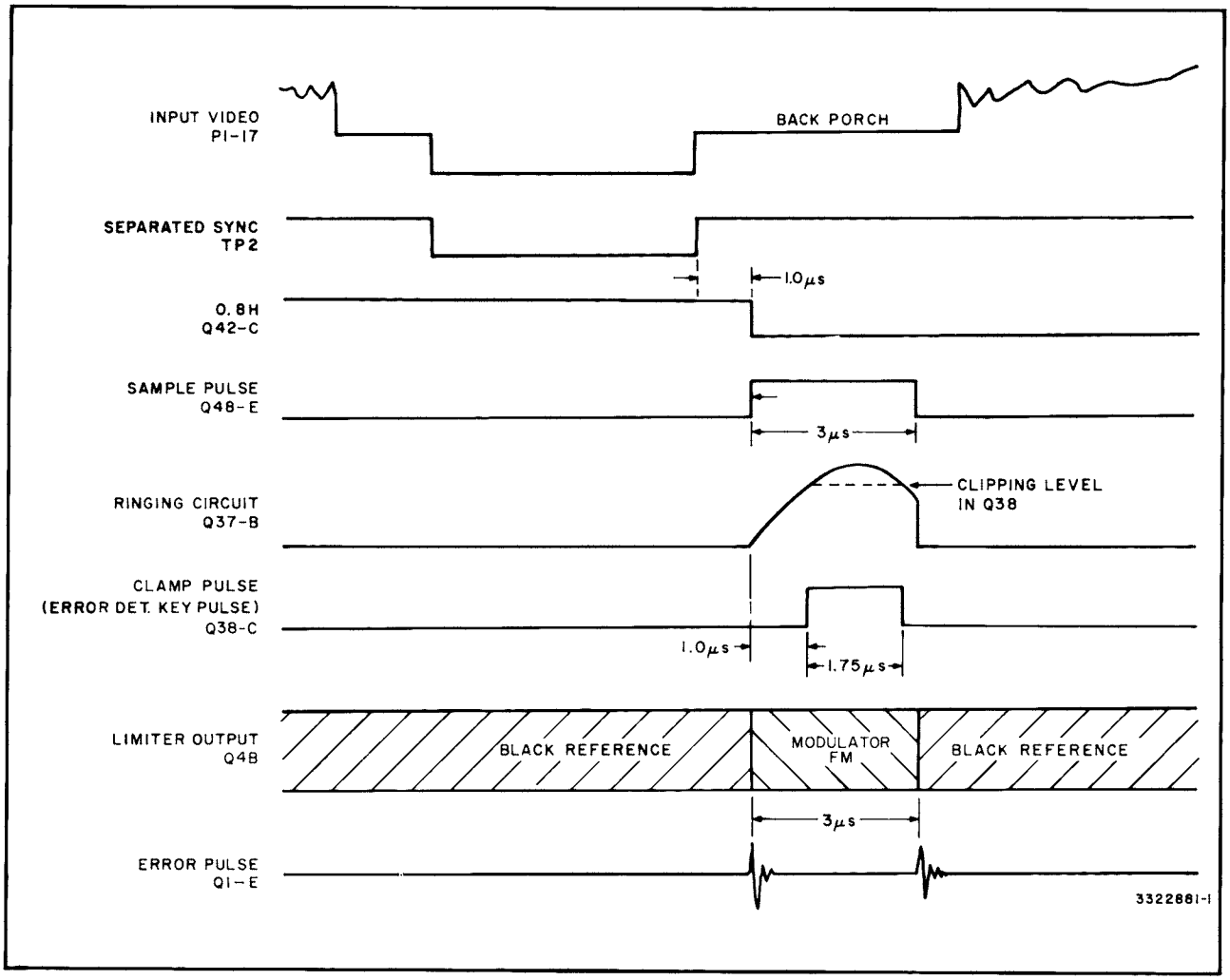


Figure 17—Modulator AFC Module, Timing Waveforms

cluded on the front panel of the module. When the switch is in OFF position, the E-E OFF indicator is illuminated (TR-22HB only). Another set of contacts on the same switch activates the audio E-E bus when the switch is placed to ON position.

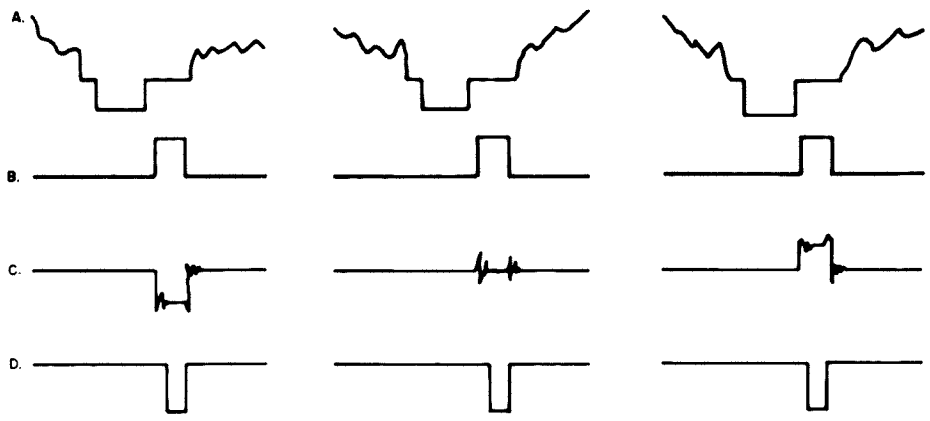
Sync Separator

Composite video input to the Modulator AFC module is supplied through pin 17 of P1 and terminated at 75 ohms with resistor R74. The signal passes through the closed contacts of relay K3, and is ac-coupled through capacitor C53 and resistor R81 to the base of transistor Q31. Refer to figure 19.

Resistor R81, in combination with capacitor C55 rolls off high-frequency response. This serves to partially shape sync transitions by removing excessive high frequency components. The resistor-capacitor network on the emitter of Q31, consisting of R84 and C56, with parallel resistor R85, serves to establish the required ac-gain of the transistor in combination with collector load resistor R83. DC bias is established by the voltage divider on the base of Q31 with reisistors R79, R80, and emitter resistor R85.

Amplified video is taken from the collector of Q31 and coupled directly to the base of succeeding amplifier transistor Q32. The collector output from the latter transistor is then coupled through emitter follower Q33. Composite video amplitude at this point is at approximately 10 volts and sync is negative-going.

Capacitor C57 and diode CR32 comprise a dc restorer that sets the negative sync tips at approximately minus 0.7 volt regardless of picture content. Resistor R89 provides base bias for transistor Q34 and also serves to charge capacitor C57 under certain signal conditions. This signal is fed to one input base of the differential amplifier and clipper using Q34 and Q35. The second input base is at ground potential, causing the emitter of Q35 to be set at approximately plus 0.3 volt; thus, Q34 emitter is also held at plus



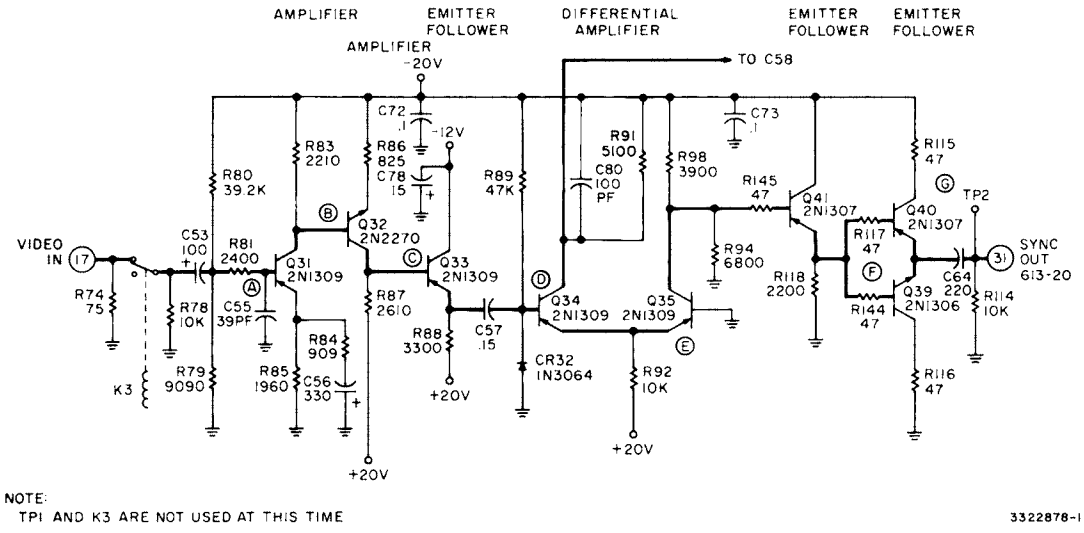
CARRIER FREQ. TOO LOW	CARRIER FREQ. CORRECT	CARRIER FREQ. TOO HIGH
A. INPUT VIDEO FOR TIMING REF.	A. INPUT VIDEO FOR TIMING REF.	A. INPUT VIDEO FOR TIMING REF.
B. SAMPLING PULSE	B. SAMPLING PULSE	B. SAMPLING PULSE
C. NEGATIVE AFC ERROR SIGNAL RESULTING FROM CARRIER FREQUENCY TOO LOW.	C. NO AFC ERROR, INDICATING CORRECT CARRIER FREQUENCY.	C. POSITIVE AFC ERROR SIGNAL RESULTING FROM CARRIER FREQUENCY TOO HIGH.
D. CLAMP PULSE DURATION.	D. CLAMP PULSE DURATION.	D. CLAMP PULSE DURATION.

NOTES:

1. THE MODULATOR MODULE DC CLAMP REFERENCE VOLTAGE IS MODIFIED DURING THE CLAMPING INTERVAL BY THE AFC ERROR SIGNAL WHICH IS SUPERIMPOSED ON IT, TENDING TO SHIFT THE CARRIER FREQUENCY TOWARD CORRECT VALUE.
2. ERROR AMPLITUDES ARE EXAGGERATED TO EMPHASIZE CORRECT PROCESS.

3321684

Figure 18—AFC Correction Waveforms



NOTE:
TP1 AND K3 ARE NOT USED AT THIS TIME

3322878-1

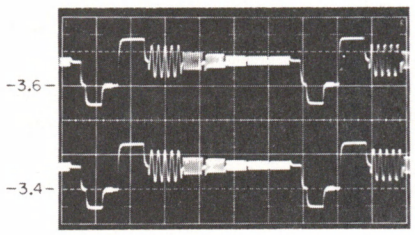
Figure 19—Sync Separation, Schematic Diagram and Typical Waveforms

0.3 volt. Transistor Q34 will conduct until its base becomes cut off if driven more positive. Therefore, the positive half of sync and the entire video amplitude range (being highly positive) cuts off Q32.

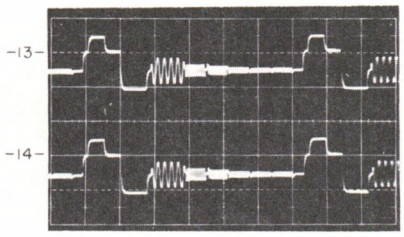
Conversely, when the signal on the base of Q34 becomes slightly more negative than its 0.3-volt emitter potential, Q34 will conduct heavily. This tends to cut off Q35 because the emitter of Q35 becomes less positive. In summary, it may be noted that transistors Q34 and Q35 function as switches that alternately cut off and conduct as sync (and video) level varies above and below the plus 0.3-volt threshold. The outputs are completely free of video and sync tip disturbances.

One output (positive-going) from the differential amplifier is supplied from the collector of Q34 to the timing generation circuit (described later). The remaining output from the differential amplifier (which is negative-going) is fed from the collector of Q35 to emitter follower Q41. The latter transistor is used to couple the clipped sync signal to the succeeding complementary symmetry emitter follower.

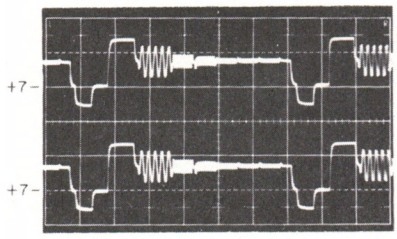
Transistors Q39 and Q40 form a complementary symmetry emitter follower circuit whose combined emitter outputs are coupled through capacitor C64



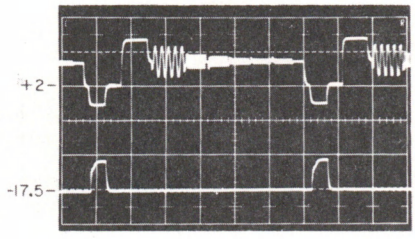
A. Top: Q31 base
Bottom: Q31 emitter
Both: .5 v/cm, 10 μs/cm



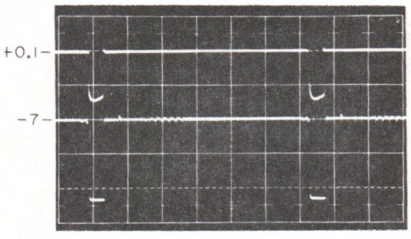
B. Top: Q32 base
Bottom: Q32 emitter
Both: 2 v/cm, 10 μs/cm



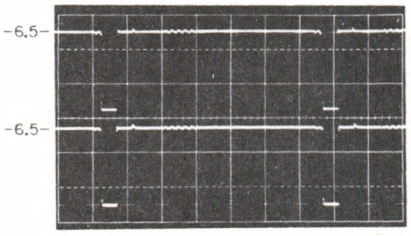
C. Top: Q33 base
Bottom: Q33 emitter
Both: 5 v/cm, 10 μs/cm



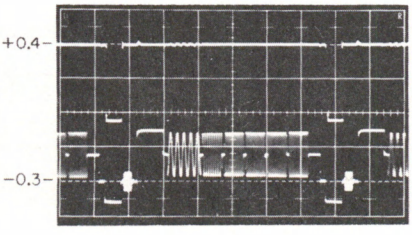
D. Top: Q34 base
Bottom: Q34 collector
Both: 5 v/cm, 10 μs/cm



E. Top: Q35 emitter, .5 v/cm
Bottom: Q35 collector, 2 v/cm
Both: 10 μs/cm



F. Top: Q41 emitter
Bottom: Junction Q39/Q40 emitters
Both: 2 v/cm, 10 μs/cm



G. Top: TP2, 2 v/cm
Bottom: 402-TP1, .5 v/cm
Both: 10 μs/cm

All waveforms in E-E mode.

Figure 19—Sync Separation, Schematic Diagram and Typical Waveforms (Continued)

and pin 31 to the Reference Generator module. This circuit configuration is sued to minimize pulse transition distortion. Resistors R115 and R116 are current limiting resistors to protect transistors Q39 and Q40 in event both transistors conduct simultaneously. Test point TP2 is provided to check the sync signal that has been separated from the input video information.

Clamp Pulse Generator

The clamp pulse generator circuit description is divided into two groups to adequately describe the two functions performed in that circuit. References to appropriate illustrations are made for each description.

Timing Circuits

The clamp pulse timing generator contains two multivibrators that establish the time rate for the positive and negative clamp pulses, and for the AFC sampling pulses. The positive-going clipped sync pulses supplied from the collector of Q34 in the differential amplifier (described previously) are accoupled through capacitor C58 and resistor R95 to the base of transistor Q36. Shunt capacitor C80 on the collector of Q34 introduces a short time delay by increasing the rise and fall times of the waveform. See figures 17 and 20.

Incoming sync pulses from the differential amplifier are amplified and inverted through Q36, and its collector output is differentiated through capacitor C59. Positive transitions at the trailing edges of the pulses then pass through triggering diode CR33, and are applied to the base of transistor Q42.

Transistors Q42, Q43, and Q44 form a monostable multivibrator whose cycling time is eight tenths of the horizontal interval (0.8 H). In its stable state, transistor Q42 is saturated by a negative base bias applied from the minus 20-volt bus through resistors R120 and R121 and forward-biased diode CR39. In this condition, the collector of Q42 is placed at ground potential which allows sufficient positive bias from the plus 20-volt supply through resistor R127, to cut off transistor Q44. The prevailing condition also cuts off transistor Q43.

Upon arrival of a positive trigger pulse to the base of Q42 from the trailing edge of sync, transistor Q42 begins to go toward cutoff and its collector po-

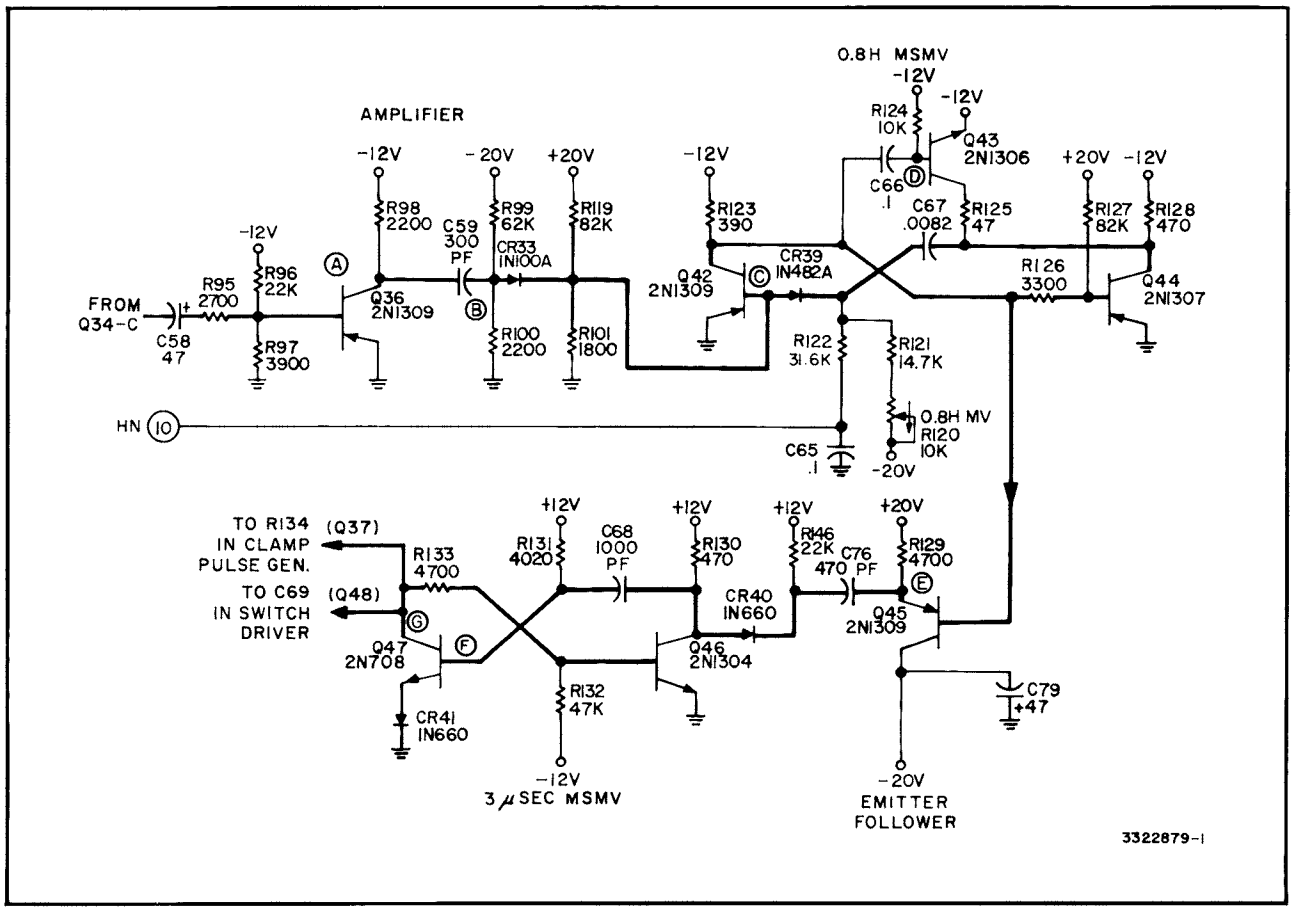
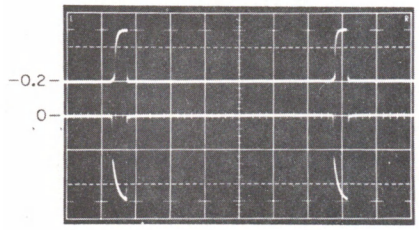


Figure 20—Timing Generator, Schematic Diagram and Typical Waveforms

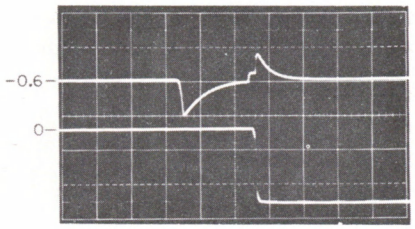
tential increases toward minus 12 volts. This causes a negative bias to be applied to the base of Q44 which causes this transistor to begin conducting. The resulting positive-going transition at the collector of Q44 (as it changes from minus 12 volts toward ground potential) is coupled through capacitor C67 and cuts off CR39, allowing the base at Q42 to rise in potential to the level established by resistor network R119/R101, reinforcing the cutoff trend occurring in transistor Q42.

The regenerative action presented by transistors Q42 and Q44 results in a rapid switch in conduction state of these two transistors, which is terminated when Q42 is completely cutoff and Q44 is fully saturated. This condition is maintained while capacitor C67 charges negatively through resistors R120, R121, and R122. During this interval, the multivibrator is immune to additional trigger pulses and noise that may cause it to reverse state.

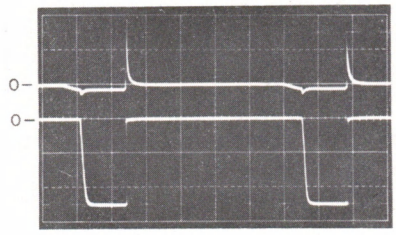
After elapse of a period of time corresponding to eight tenths of the horizontal rate, capacitor C67 is charged sufficiently to cause the base of Q42 to become forward biased through diode CR39. Transistor Q42 now begins conducting and its collector



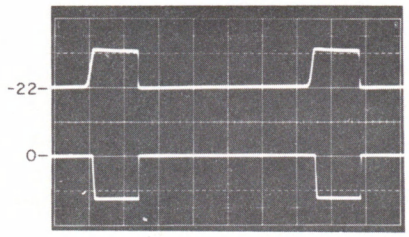
A. Top: Q36 base, 1 v/cm
Bottom: Q36 collector, 5 v/cm
Both: 10 μs/cm



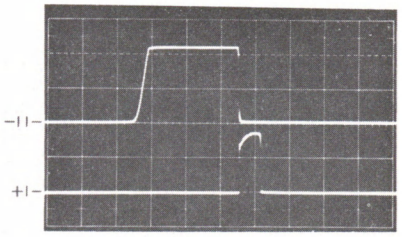
B. Top: Junction R99/R100
Bottom: Q42 collector
Both: 5 v/cm, 2 μs/cm



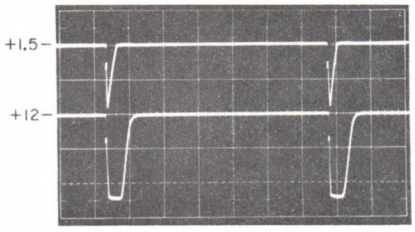
C. Top: Q42 base
Bottom: Q44 collector
Both: 5 v/cm, 10 μs/cm



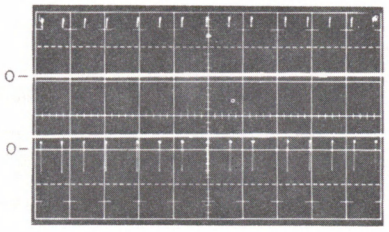
D. Top: Q43 base
Bottom: Q43 collector
Both: 10 v/cm, 10 μs/cm



E. Top: Q45 emitter
Bottom: Q47 collector
Both: 5 v/cm, μs/cm



F. Top: Q47 base
Bottom: Q46 collector
Both: 5 v/cm, 10 μs/cm



G. Top: Q47 collector, 5 v/cm
Bottom: Q47 emitter, 2 v/cm
Both: 100 μs/cm
UNITY/VAR switch to UNITY

All waveforms in E-E mode.

Figure 20—Timing Generator, Schematic Diagram and Typical Waveforms (Continued)

potential drops toward ground level. The positive transition on the collector of Q42 is coupled through R126 and cuts off Q44, which brings the collector of Q44 toward minus 12 volts. Simultaneously, the positive pulse from the collector of Q42 is coupled through capacitor C66, causing transistor Q43 saturate, thereby connecting capacitor C67 directly to minus 12 volts and increasing the transition speed over that resulting from the cutoff of Q44 alone.

The above condition results in a negative pulse that occurs shortly after trailing edge (TE) of sync, and lasts approximately 50 microseconds on 525 or 625 line standards, or 80 microseconds on 405 line standards. Changes in time duration is accomplished by the horizontal-normal (HN) bus which is at minus 20 volts for 525/626 line standards, but is at ground potential for 405 line standard.

Because of the differences in potential of the HN bus, current available for recharging capacitor C67 is much higher on 525/626 line standards when the HN bus is negative while the minus-20 volt bus is normally available. Therefore, the capacitor charges more rapidly than when operating in 405 line standard, when the current source is available only from the minus 20-volt bus. Adjusting potentiometer R120 for a multivibrator period of 50 microseconds while in 525/625 line standards, automatically places the period of the multivibrator close to 80 microseconds when operation is selected for 405 line standards.

Each time the 0.8 H multivibrator is cycled, pulses are supplied to the base of emitter follower Q45. These pulses are then differentiated through capacitor C76, and the negative-going leading-edge transistions are fed to the three-microsecond multivibrator (Q46/Q47). This is a monostable type multivibrator that operates in a manner similar to that described for the 0.8H multivibrator except that the time constant of this multivibrator causes a three-microsecond pulse to be supplied from the collector of Q47. The leading edge of this pulse occurs during the back-porch interval, approximately one microsecond later than the trailing edge of the horizontal sync pulse on the composite video input signal. The one-microsecond delay represents the accumulations of delays in the sync separation process, rolloff effect of capacitor C80, and multivibrator triggering. The pulse is then supplied to the ringing circuit of the clamp pulse generator circuit, and to emitter follower Q48 that drives the sampling switch (both in the AFC switching circuit), which is described below.

Clamping Circuits

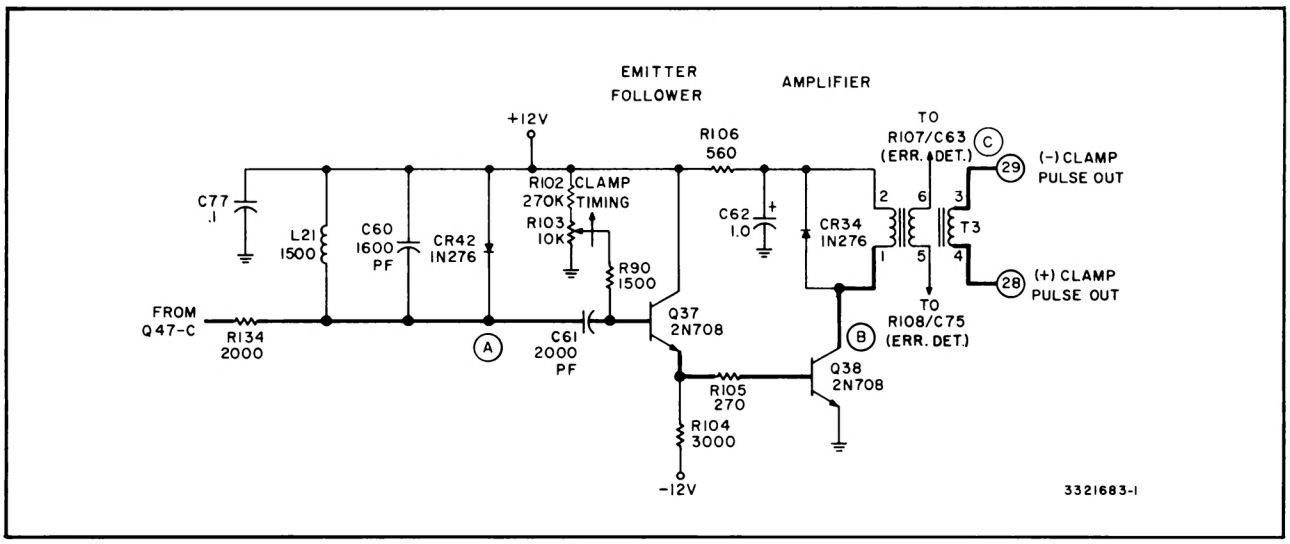
The collector output from Q47 is supplied through resistor R134 to a ringing circuit using inductor L21 and capacitor C60. Energy in the leading edge of the positive-going pulse excites L21 and C60 into oscillation at a frequency determined by resonance between the inductor and capacitor. Normally, this would cause a train of sine waves with decreasing amplitude to be formed. However, after the first positive half cycle is generated, and the sine wave begins to go negative, diode CR42 conducts to discharge capacitor C60 and end the oscillation. The ringing circuit now remains inoperative until arrival of the next excitation pulse. The pulses thus generated are positive, partial half-sine waves with a baseline width of approximately three microseconds and an amplitude of two volts. Refer to figures 17 and 21.

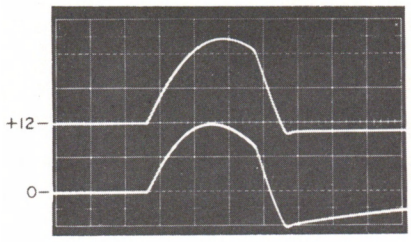
Positive, half-sine waves are ac-coupled through capacitor C61 to the base of transistor Q37, which is an emitter follower that drives the base of Q38. An adjustable voltage divider using resistors R102 and R103, and which is coupled to the base of Q37 through resistor R90, adds a dc component to the half-sine wave signal to permit precise adjustment for conduction of transistor Q38. The bias is adjusted so that only the tip of the half-sine wave signal drives Q38 into a conducting state. This generates a rectangular current pulse through Q38 with a leading edge delayed approximately one microsecond from the initiation of the half-sine wave. The current pulse is completed prior to completion of the half-sine wave. This pulse is 1.75 microseconds wide, and occurs within the time limitations of the three-microsecond pulse supplied from the collector of Q47 to the base of Q37. Precise width and position of the square-wave pulse is controlled by clamp timing potentiometer R103.

The collector output from Q38 is a train of negative-going pulses that drive the primary winding of transformer T3. The latter has two secondary windings. One secondary winding supplies the positive and negative clamping pulses through pins 28 and 29, respectively, to the Modulator module clamp circuit. The second winding of T3 secondary is supplied to an AFC error detector bridge in this module. Diode CR34 suppresses the positive spike that would otherwise be developed by the sudden current change in transformer T3.

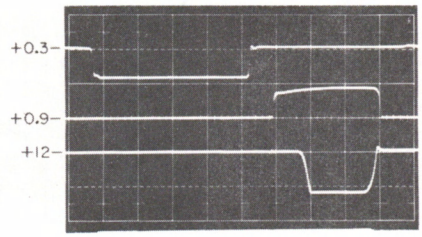
AFC Switching

AFC switching is accomplished before the input to transformer T1. Switching is controlled by the

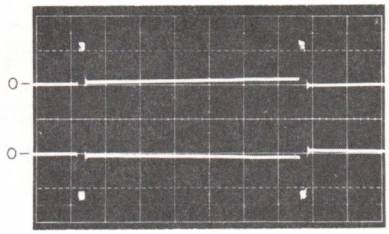




A. Top: Junction R134/CR42/C61
Bottom: Q37 base
Both: 1 v/cm, 1 μs/cm



B. Top: TP2, 5 v/cm
Middle: Q47 collector, 10 v/cm
Bottom: Q38 collector, 10 v/cm
All: 1 μs/cm



C. Top: P1 pin 28
Bottom: P1 pin 29
Both: 5 v/cm, 10 μs/cm

All waveforms in E-E mode.

Figure 21—Clamp Circuit, Schematic Diagram and Typical Waveforms

three-microsecond sampling pulse supplied from the three-microsecond multivibrator (Q46/Q47) in the timing generator circuit. Refer to figures 17 and 22.

As described previously, three-microsecond sampling pulses at the horizontal rate are supplied from the three-microsecond multivibrator (Q46/Q47). These pulses are ac-coupled through capacitor C69 and applied to the base of Q48. The latter is an emitter follower which couples the three-microsecond, positive-going pulses to the center-tap of the primary winding of transformer T1 through isolation resistor R138. Resistors R135 and R136 bias Q48 so that the emitter voltage varies between plus 6.0 volts at the tip of the pulse and minus 2.5 volts at the pulse base. These pulses cause diodes CR11 and CR12 to be switched "on" and "off" at the pulse rate and at the time limitations of each incoming pulse, thus controlling the switches connected to the outer ends of the primary winding.

One input to the switch is the black reference signal supplied from the black reference crystal-controlled oscillator in the FM Reference module. This signal is fed into the module through pin 21 and is applied to the base of transistor Q10. The transistor serves to isolate the switching circuit from the black reference signal input line. The emitter output from Q10 is ac-coupled through capacitor C26 to the electronic switch consisting of diodes CR11A and CR12A.

The second switch input is an FM output signal supplied from the Modulator module through pin 19 and applied to the base of transistor Q20. This is an emitter follower which is cascaded with transistor Q19 to isolate the incoming signal from the electronic switch that follows. The emitter output from Q19 is ac-coupled through capacitor C33 to the second electronic switch, consisting of diodes CR11B and CR12B.

With each electronic switch connected to opposite ends of the primary winding of the transformer, and the input diodes of each switch connected in opposite polarity, the transformer will accept an input from either end of the primary winding according to the level presented into the center tap. Thus, the sampling pulses supplied from the three-microsecond multivibrator determine which signal passes through transformer T1.

Each three-microsecond, positive-going sampling pulse supplied to the center tap of T1 causes diode CR11B to become forward biased, while causing diode CR12B to become reverse biased. This causes FM from the Modulator module to pass through the transformer. Simultaneously, the reference signal path is blocked because diode CR12A is reverse biased and CR11A is forward biased. The conduction of CR11A incidently grounds one end of the trans-

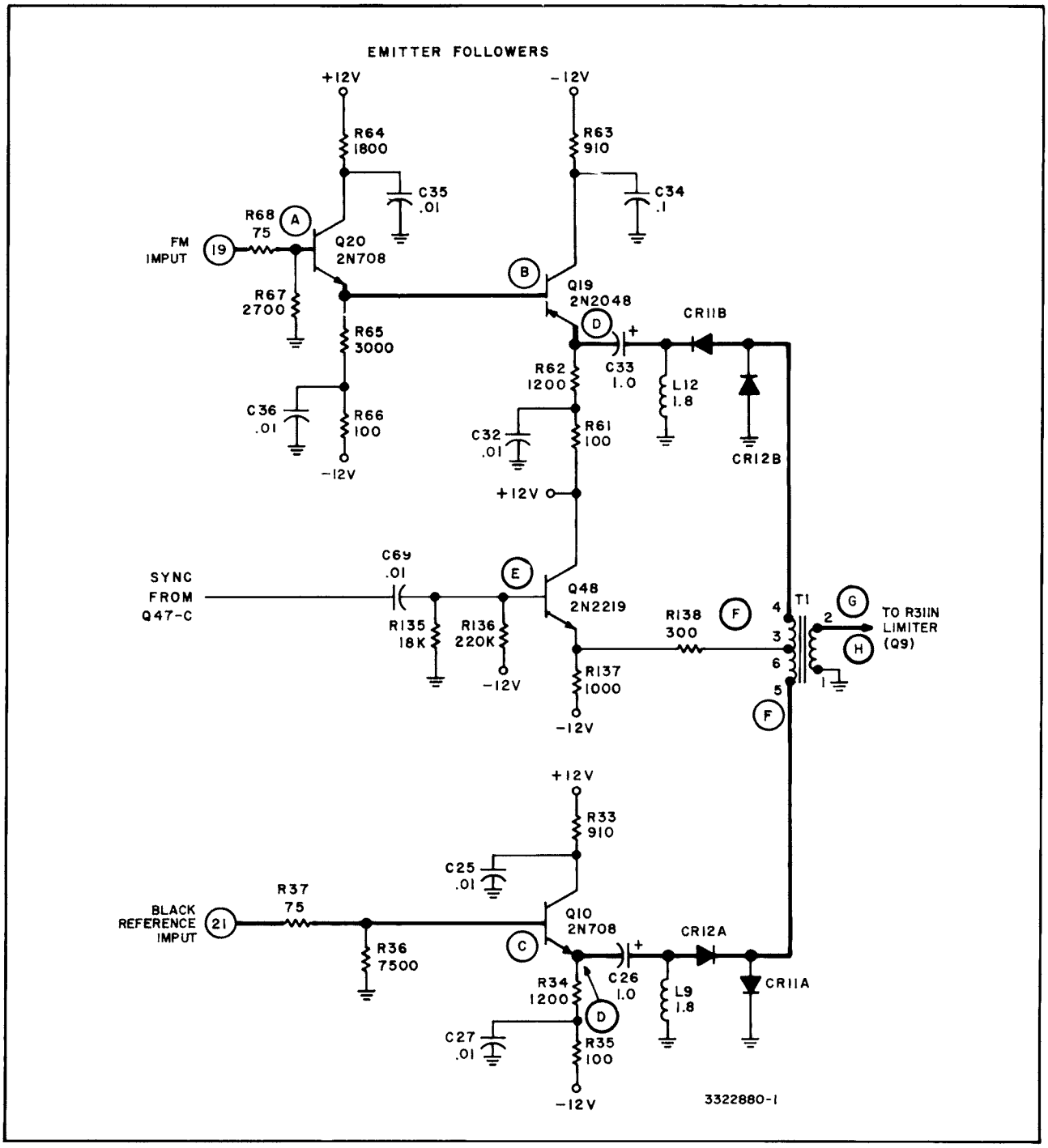
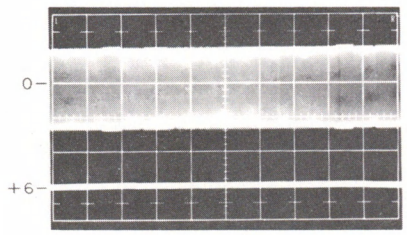


Figure 22—AFC Switching, Schematic Diagram and Typical Waveforms

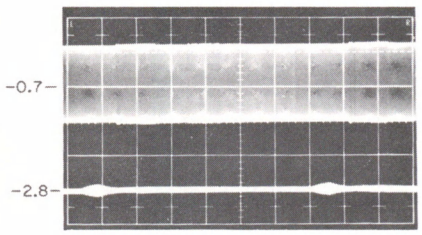
former primary winding for proper operation with the presently-active fm switch.

Conversely, when the negative portion of the sampling pulse occurs (approximately 60 microseconds in a 525/625 line standard), diode CR11B is reverse biased and CR12B is forward biased, thus interrupting the Modulator fm signal path to T1. During this interval, however, CR12A is forward biased and CR11A is cut off, permitting the black reference signal to pass through the transformer. The primary of the transformer is thus switched sequentially from the reference signal to the Modulator fm for three-microsecond intervals during the back porch time. Frequency differences between the two components of the switch output are subsequently detected and applied to the Modulator clamp reference for automatic frequency control.

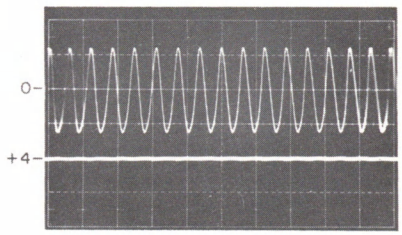
Inductors L9 and L12 furnish a dc path to ground for diode biasing, but have sufficient reactance to avoid affecting the rf signals. Balanced diodes are used at CR11A and CR11B and at CR12A and CR12B to assure cancellation of the sampling pulse in the primary of T1.



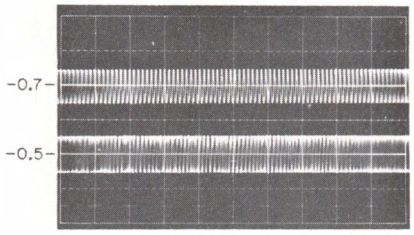
A. Top: Q20 base
Bottom: Q20 collector
Both: .2 v/cm, 10 μs/cm



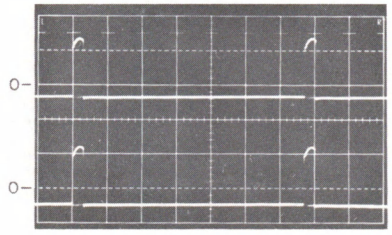
B. Top: Q19 base
Bottom: Q19 collector
Both: .2 v/cm, 10 μs/cm



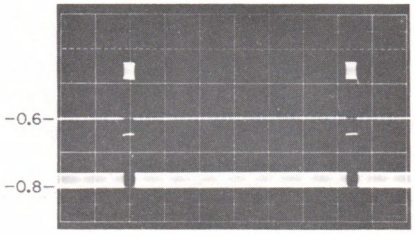
C. Top: Q10 base, .2 v/cm
Bottom: Q10 collector, .5 v/cm
Both: .2 μs/cm



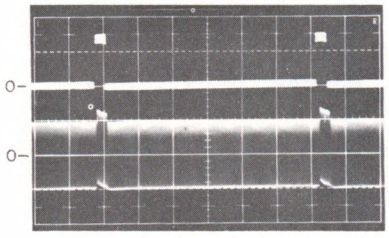
D. Top: Q10 emitter
Bottom: Q19 emitter
Both: .5 v/cm, 1 μs/cm



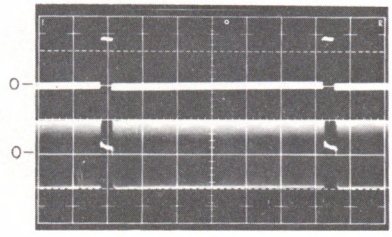
E. Top: Q48 base
Both: Q48 emitter
Both: 5 v/cm, 10 μs/cm



F. Top: T1 pin 5
Bottom: T1 pin 4
Both: 1 v/cm, 10 μs/cm



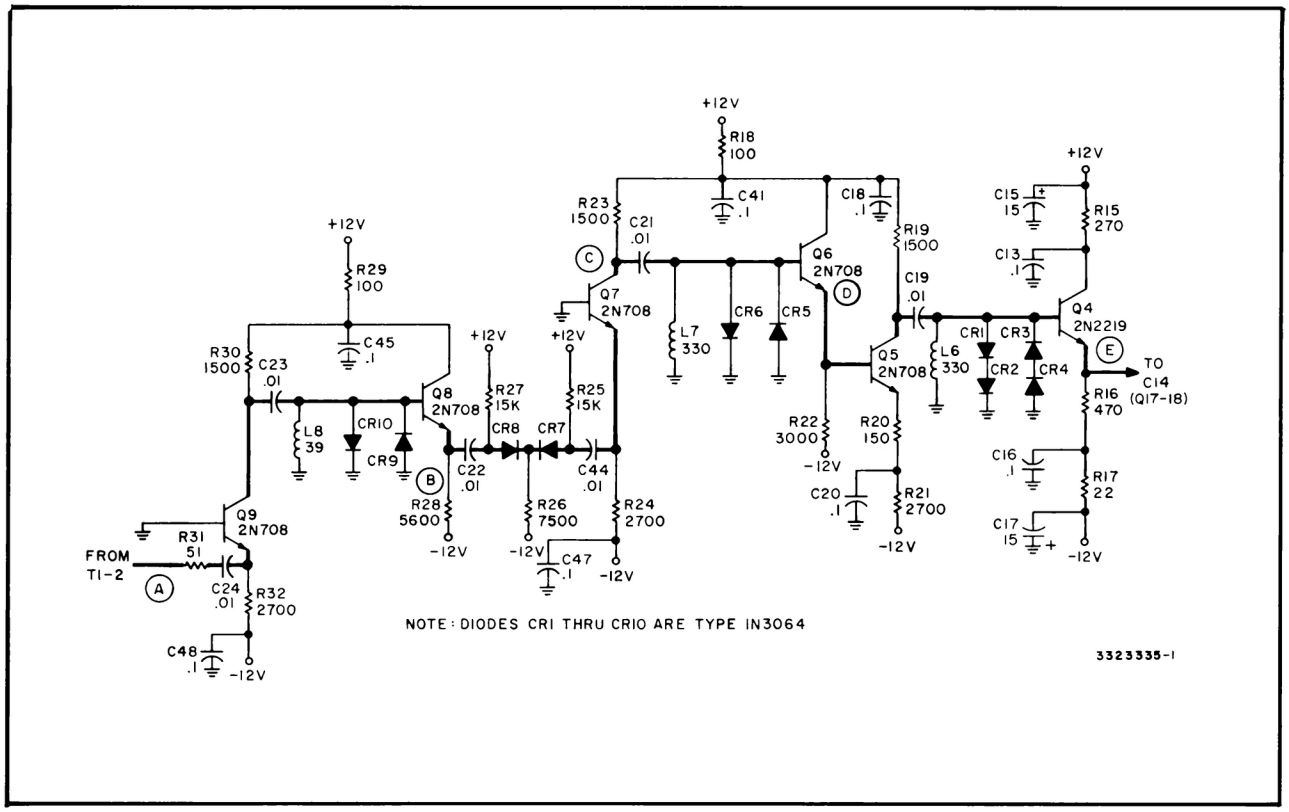
G. Top: T1 junction 3/6 pins
Bottom: T1 pin 2
Both: .1 v/cm, 10 μs/cm

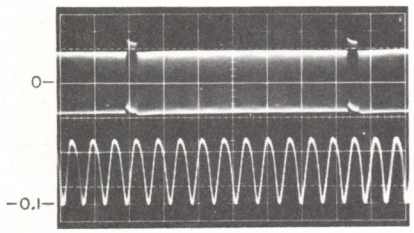


H. Top: T1 junction 3/6 pins
Bottom: T1 pin 2
Both: .1 v/cm, 10 μs/cm
Modulator module (510) removed

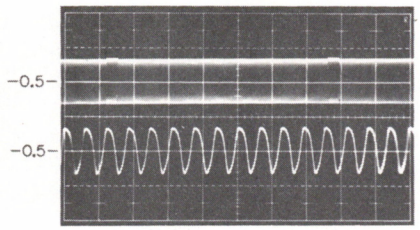
All waveforms in E-E mode.

Figure 22—AFC Switching, Schematic Diagram and Typical Waveforms (Continued)

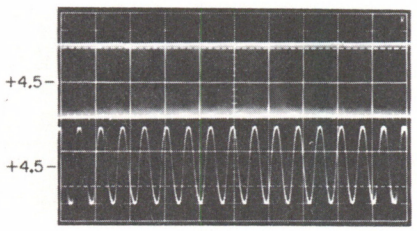




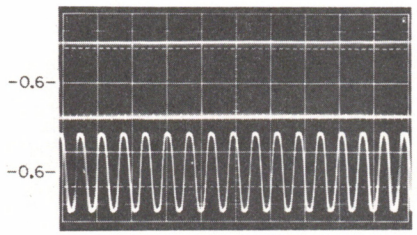
A. Top: R31, 10 μs/cm
Bottom: R31, .2 μs/cm
Both: .1 v/cm



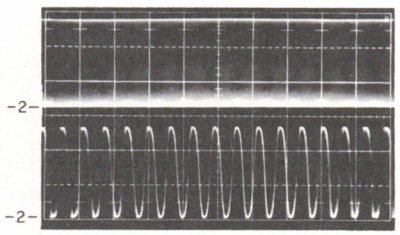
B. Top: Q8 emitter, 10 μs/cm
Bottom: Q8 emitter, .2 μs/cm
Both: 1 v/cm



C. Top: Q7 collector, 10 μs/cm
Bottom: Q7 collector, .2 μs/cm
Both: .5 v/cm



D. Top: Q6 emitter, 10 μs/cm
Bottom: Q6 emitter, .2 μs/cm
Both: .5 v/cm



E. Top: Q4 emitter, 10 μs/cm
Bottom: Q4 emitter, .2 μs/cm
Both: 1 v/cm

All waveforms in E-E mode.

Figure 23—AFC Limiter, Schematic Diagram and Typical Waveforms

AFC Limiter

Switched FM and black reference signals are clipped through a four-stage limiter prior to demodulation within the module. The secondary winding of transformer T1 supplies its output through load resistor R31 to the emitter of grounded-base amplifier transistor Q9. The amplified output from its collector is then limited with shunt diodes CR9 and CR10 for the first of four succeeding limiter stages which are used to provide identical amplitude of the sequential Modulator fm and black reference signals. Refer to figure 23.

Transistor Q8 is an emitter follower that couples the signal to a series limiter stage using diodes CR8 and CR7. Diode CR8 is biased "on" by resistors R26 and R27. The diode remains conducting, passing the signal, until the level of the negative half-cycles exceeds the diode-conduction voltage. The diode is then cut off to block the signal flow. Diode CR7 serves a similar function; clipping positive half-cycles. The signal is now amplified with grounded-base amplifier transistor Q7 which presents a desired low impedance to the series limiter. Third-stage limiting is with diodes CR5 and CR6. Emitter follower Q6 couples the signal from the third limiter to amplifier Q5. Final limiting is with diodes CR1 through CR4, after which the signal is coupled through emitter follower Q4 to the AFC demodulation circuits. Two diodes in series for each branch of this limiter stage assures sufficient signal level to drive the demodulator stage that follows.

AFC Demodulation

Output from the final limiter stage at transistor Q4 is ac-coupled through capacitor C14 at the high-frequency equalizing circuit using inductor L11 and resistor R60. The signal is then applied to autotransformer T2 which drives the AFC balanced demodulator using transistors Q17 and Q18. Refer to figure 24.

The rf square waves from the limiter are differentiated by capacitor C14, resulting in narrow, constant-width pulses for each transition of the square waves. A positive pulse is generated by the positive-going square-wave transition, and a negative pulse by each negative-going transition. Pulses applied to the autotransformer are coupled in push-pull to drive the bases of Q17 and Q18, so that when one base is driven positive, the other is negative, and vice versa. Only the negative pulses can cause the PNP type transistors to conduct, thus the two transistors conduct alternately as each is driven by the negative pulses.

The output produced is a positive pulse of constant width from the collector of the conducting transistor. Outputs from both collectors (Q17 and

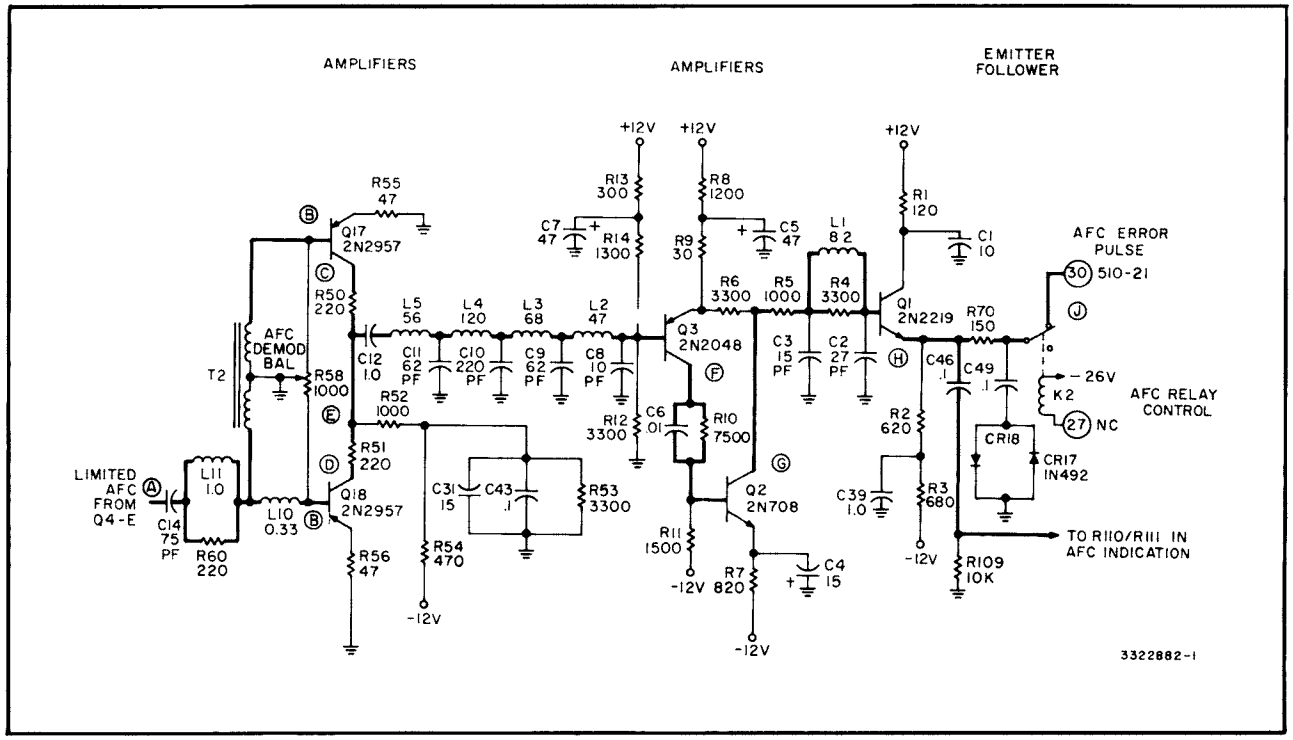
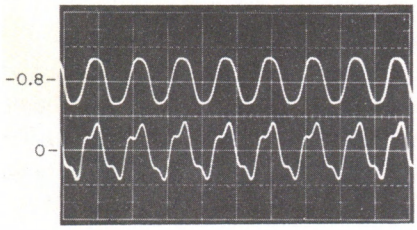


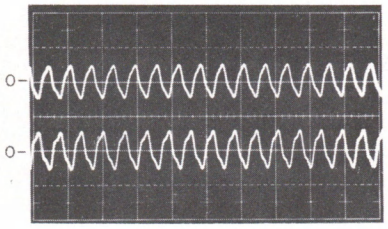
Figure 24—AFC Demodulation, Schematic Diagram and Typical Waveforms

Q18) are combined in resistors R51 and R52 to produce at their junctions a train of constant-width pulses with each pulse representing an input rf transition. Inductor L10 provides compensating delay to match that produced through autotransformer T2 so that pulses arrive at the transistor bases simultaneously.

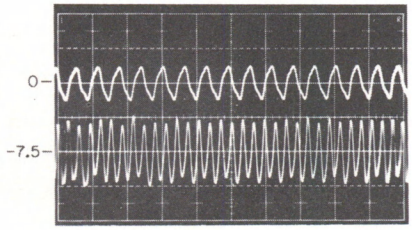
The combined outputs from transistors Q17 and Q18 is coupled through a low-pass filter consisting of inductors L2 through L5 and capacitors C8 through C11. The filter has a cutoff considerably below the fm carrier frequency so that the output of the filter corresponds only to the *average* input energy. Because each input pulse has a constant level of energy, the filter output depends on only the rate (frequency) of input pulses. The higher the frequency, the more positive becomes the output. Thus, the constant-width pulse generator feeding the lowpass filter comprise a detector capable of converting input frequency variations to output level variations. Potentiometer R58 permits adjustment of relative input drive levels for optimum output symmetry.



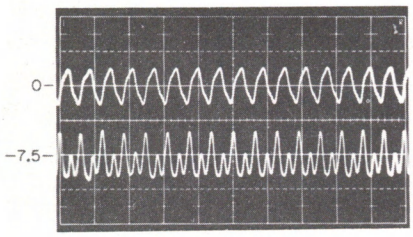
A. Top: C14, 2 v/cm
Bottom: Junction C14/L11/R60, 1 v/cm
Both: .1 μs/cm



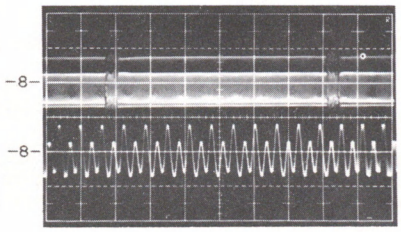
B. Top: Q17 base
Bottom: Q18 base
Both: 1 v/cm, .2 μs/cm



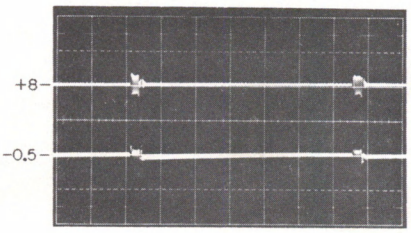
C. Top: Q17 base
Bottom: Q17 collector
Both: 1 v/cm, .2 μs/cm



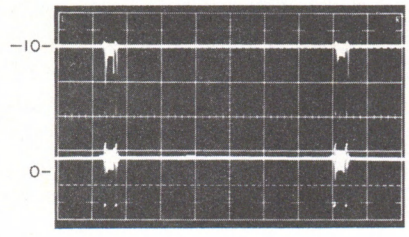
D. Top: Q18 base, 1 v/cm
Bottom: Q18 collector, 2 v/cm
Both: .2 μs/cm



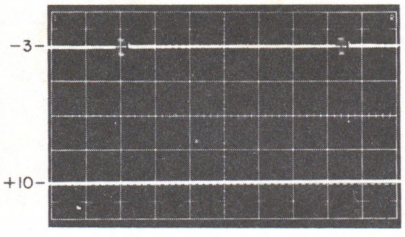
E. Top: Junction R50/R51/R52, 10 μs/cm
Bottom: Junction R50/R51/R52, .2 μs/cm
Both: 1 v/cm



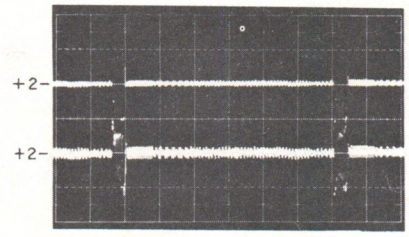
F. Top: Q3 base, .1 v/cm
Bottom: Q3 collector, .2 v/cm
Both: 10 μs/cm



G. Top: Q2 base, 1 v/cm
Bottom: Q2 collector, 10 v/cm
Both: 10 μs/cm



H. Top: Q1 base, 5 v/cm
Bottom: Q1 collector, 2 v/cm (dc)
Both: 10 μs/cm



J. Top: Q1 emitter, 2 v/cm
Bottom: P1 pin 30, 1 v/cm
Both: 10 μs/cm

All waveforms in E-E mode.

Figure 24—AFC Demodulation, Schematic Diagram and Typical Waveforms (Continued)

A change in the input frequency can exist only during a three-microsecond interval when the Modulator FM differs from the reference frequency. Any difference in these two frequencies results in a three-microsecond error pulse from the filter. The pulse polarity depends on the direction of frequency error, and its amplitude depends on the magnitude of error. The pulse is developed across filter-terminating resistors R12 and R14. These resistors also bias input stage Q3 of feedback amplifier Q3/Q2. Feedback amplifier gain is established primarily by the ratio of resistors R6 to R9, and is approximately 100. The amplified error signal is filtered again in C2, C3, L1 and R4 prior to application to the base of output emitter follower Q1.

The main signal path of the AFC error is from the emitter of Q1 through resistor R70 and the normally-closed contacts of relay K2 to pin 30 of P1. Back-to-back diodes CR17 and CR18 that shunt the output side of R70, clip excessive error-pulse amplitude to prevent driving the Modulator into an abnormal correction mode. Relay K2 is utilized to disable the Modulator AFC function during the noise test mode. A secondary path of the AFC error signal is supplied to the MOD FREQ indicator circuit, and is described below.

AFC Indication

Demodulated AFC signals are supplied to the AFC indication circuit as well as to the primary signal path to the Modulator module. The AFC indication circuit causes the illumination of the MOD FREQ warning indicator on the machine to indicate when the AFC error is within 8 to 25 kHz. Refer to figure 25.

AFC error at the junction of capacitor C46 and resistor R109 is supplied to the clamping bridge using diodes CR35 through CR38. Clamp pulses supplied from transformer T3 in the clamp circuit (described previously) supply positive and negative pulses having a 1.75-microsecond width. The start of the clamp pulse begins after the three-microsecond error pulse is received, and ends before the three-microsecond pulse is concluded. This prevents start and stop transients present on the error pulse from interfering with the clamp bridge operation.

When a negative pulse from transformer T3 is coupled through capacitor C63 to the cathodes junction of diodes CR36 and CR35, the diodes become forward biased. Simultaneously, a positive pulse is coupled through capacitor C75 to the anodes junction of diodes CR38 and CR37 to forward bias those diodes. This causes the entire bridge to operate as a closed switch which permits the AFC error to pass from the junction of resistors R110 and R111 to the junction of R112 and R113.

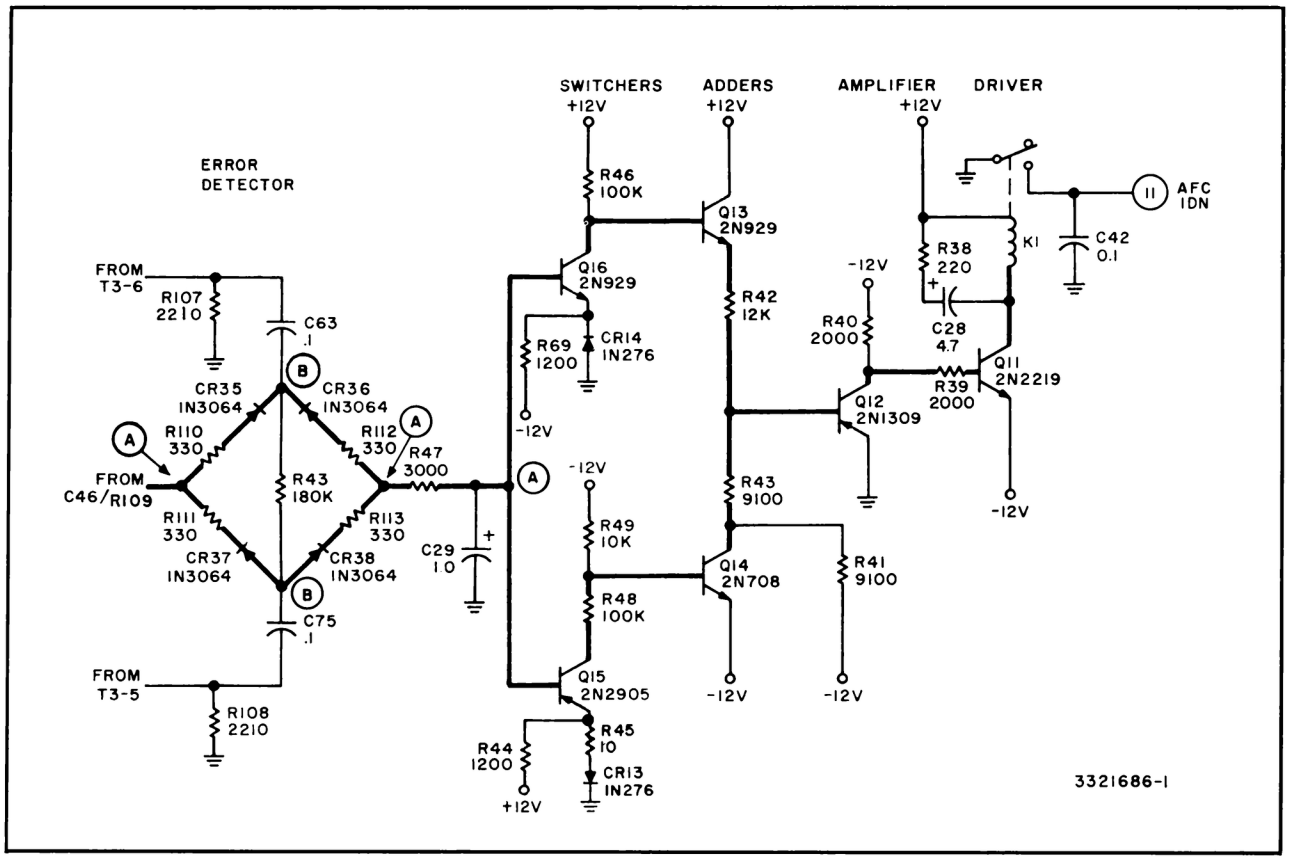
After passing through the bridge, the AFC error pulse is supplied through resistor R47 to the parallel bases of transistors Q15 and Q16. Capacitor C29 with resistor R47 form an RC network that causes the capacitor to charge toward the maximum error level, thereby providing a smoothing effect for the output of the bridge. Resistor R47 limits peak current during the charging of capacitor C29.

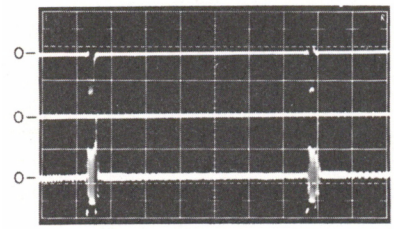
Either a positive or negative error of sufficient potential, applied to the bases of Q15 and Q16 causes relay K1 to become energized and presents an AFC error indication. If a positive error is received, NPN type transistor Q16 conducts and causes its collector to go toward ground potential due to the pre-bias effect produced with diode CR14 on the emitter of Q16. With the less-negative potential from the collector of Q16 transferred to the base of emitter follower Q13, that transistor provides a near-ground level from its emitter and places the upper end of resistor R42 to the same level.

Positive error pulses applied to the base of PNP type transistor Q15 cause that transistor to cut off. The resulting minus 12 volts on its collector is transferred to the base of amplifier transistor Q14 and also cause that transistor to cut off. Thus, a voltage divider network consisting of series resistors R42, R43, and R41 connect minus 12 volts at one end of R41, and near-ground at the opposite end of R42. This presents a negative potential on the base of Q12 to cause it to conduct. Diodes CR13 and CR14 provide temperature compensation for their respective transistor circuits, and reduce the voltage input level required to cause the transistors to conduct.

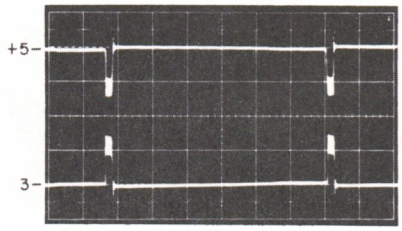
Negative error pulse cause an opposite effect through switch Q16/Q15 and adder Q13/Q14, but still provide a negative level on the base of Q12. A negative pulse causes PNP type transistor Q15 to conduct and place its collector at near-ground potential due to the pre-bias effect of diode CR13 on the emitter of Q15. A near-ground level is then transferred to the base of Q14 which now saturates and effectively shorts out resistor R41 by placing its collector at minus 12 volts.

Negative error pulses applied to the base of NPN type Q16 cause that transistor to cut off and place a plus 12-volt potential on the base of Q13. With the latter operating as an emitter follower, the plus 12 volts is presented on its emitter. A voltage divider





A. Top: Junction R112/R113, 1 v/cm
Middle: Junction C29/R47, 1 v/cm
Bottom: Junction R110/R111, 2 v/cm
All: 10 μs/cm



B. Top: Junction CR35/CR36
Bottom: Junction CR37/CR38
Both: 5 v/cm, 10 μs/cm

All waveforms in E-E mode.

Figure 25—AFC Indication Circuit, Schematic Diagram and Typical Waveforms

now exists with plus 12 volts on the upper end of resistor R42, which is in series with resistor R43, and minus 12 volts at the lower end of R43. Thus, a negative potential is presented at the base of Q12 because of the higher resistor value of R42 compared to the value of R43, and transistor Q12 is again caused to conduct.

Normally, no AFC error exists and therefore no biasing pulses are applied to the bases of Q16 and Q15, consequently both transistors are cut off. When transistor Q15 is cut off it presents minus 12 volts on the base of Q14 and causes the latter to also become cut off. However, transistor Q16 being cut off presents plus 12 volts on the base of Q13 and therefore plus 12 volts on its emitter. Thus, a voltage divider is now formed with series resistors R42, R43, and R41, in which plus 12 volts is presented at the upper end of R42 and minus 12 volts at the lower end of R41. This provides a positive potential on the base of Q12 due to the higher resistance value of R41 plus R43 compared with R42. Transistor Q12 is thereby cut off.

Assume that either a positive or negative AFC error exists and transistor Q12 conducts. Its collector then becomes more positive and transfers this potential to the base of driver transistor Q11. The latter now conducts to cause relay K1 to become energized and connect illuminating current through MOD FREQ indicator for AFC error indication. In normal operating conditions, when the AFC error is negligible, Q12 is cut off and its collector is at −12 volts. This negative level coupled through resistor R39, causes Q11 to cut off thereby deenergizing relay K1 and extinguishing the MOD FREQ indicator lamp.

E-E Switch

The E-E switch on the Modulator AFC module front panel is completely unassociated with other functions on the module. The switch serves to supply the E-E control bus to the machine by connecting the standby/wind/stop bus through the switch when the switch is positioned to ON. Placing the switch to the OFF position illuminates the E-E OFF indicator on the machine indicator panel and disables the E-E bus.

A separate set of contacts on the E-E switch supplies the audio E-E controls bus by connecting minus 26 volts through those switch contacts (TR-22HB only). Placing the switch to the OFF position illuminates the E-E OFF indicator on the machine indicator panel (TR-22HB only). The conditions resulting from the ON and OFF positions of the E-E switch are listed in the following table.

TABLE 4—E-E SWITCH OPERATING CONDITIONS

Operating Mode	*E-E ON*		*E-E OFF*	
	E-E Bus	*E-E Indicator*	*E-E Bus*	*E-E Indicator*
STOP	Gnd.	Off	Open	On
WIND	Gnd.	Off	Open	On
ST BY	Gnd.	Off	Open	On
PLAY	−26V	Off	Open	Off
SET UP	−26V	Off	Open	Off
RECORD	−26V	Off	Open	Off

ADJUSTMENTS

The Modulator AFC module has been carefully adjusted at the factory and should not be disturbed unless positive determination is made that an adjustment is required. Adjustment procedures are described for 0.8-horizontal multivibrator potentiometer R120, and clamp pulse potentiometer R103.

Demodulator balance potentiometer R58 requires special test equipment for adjustment and should not be disturbed. This control has been locked at its proper setting with red or blue sealing compound. If adjustment is required, contact your RCA representative.

0.8-Horizontal Multivibrator Adjustment

This adjustment provides for a negative pulse width of 50 microseconds on the output of the 0.8-horizontal rate multivibrator. Proceed as follows:

1. Connect the Modulator AFC module to its slot through an extender.

2. Connect a multiburst input signal to the Video Input jack on the machine.

3. Connect the oscilloscope trigger input to the VERT (TP3) test point on the Reference Generator module. Set the oscilloscope for delayed sweep.

4. Place the machine in 525 or 625 line standard operation.

5. Connect the oscilloscope input probe to the emitter of transistor Q45.

6. Adjust potentiometer R120 on the Modulator AFC module for a negative pulse width of 50 (±1.0) microseconds.

NOTE: On machines operating with 405 line standards. The pulse width should be 80 (±8) microseconds when 405 line standard operation is selected.

Clamp Pulse Adjustments

This adjustment sets the pulse width and delay of

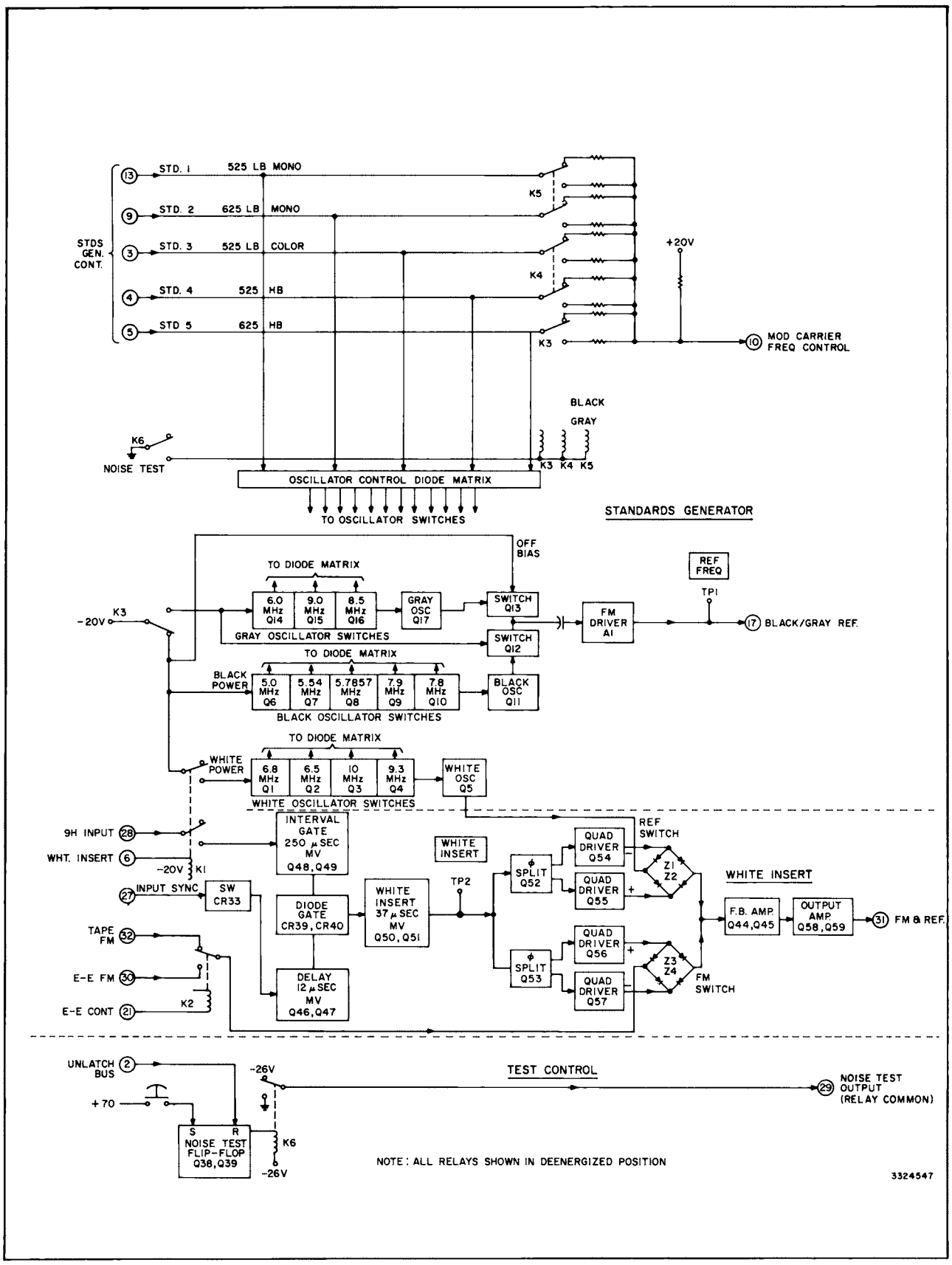


Figure 26—FM Reference Module, Block Diagram

the clamp pulse supplied from the collector of driver transistor Q38. Proceed as follows:

1. Connect the Modulator AFC module to its slot through an extender.

2. Connect a multiburst input signal to the Video Input jack on the machine.

3. Connect the oscilloscope trigger input to the VERT (TP3) test point on the Reference Generator module. Set the oscilloscope dual-channel pre-amplifier for alternate sweep.

4. Connect one input probe of the oscilloscope to the emitter of transistor Q48, and the other input probe to the collector of Q38.

5. Adjust clamp timing control potentiometer R103 for a pulse width of 1.75 microseconds.

NOTE: After the adjustment is accomplished, the clamp pulse leading edge at the collector of Q38 should be delayed from the sampling pulse leading edge at the emitter of Q48 by 1.1 ($\pm$0.1) microseconds. Also, the clamp pulse trailing edge should preceed the sampling pulse trailing edge by at least 0.1 microsecond.

FM REFERENCE MODULE

CIRCUIT DESCRIPTION

General

The FM Reference module ensures that recordings are made according to established standards. The module is also part of the machine's built-in test equipment. As illustrated on the block diagram, figure 26. Three basic purposes are served as follows:

1. *Standards Reference.* Supplies a dc voltage to the Modulator module, that is related to the machine operating standard and will control the modulation frequency according to the selected standard. This function also generates crystal-controlled standard test frequencies to coincide with gray, black, and white signals according to the selected operating standard.

A negative 20 volts is supplied from the Standards Generator module to one of five inputs on the FM Reference module. The particular input supplied is determined by selection of one of five operating standards. Once inside the module, the minus 20 volts is fed in parallel to the oscillator control diode matrix and to one center arm of relay K5, K4, or K3.

Each of the fixed contacts of relays K5, K4, and K3 are connected to precision resistors. The minus 20 volts is thus fed through the particular resistor associated with the selected standard which forms a voltage divider with another precision resistor that is common to all the selected resistors. The opposite end of the common resistor is permanently connected to positive 20 volts, therefore a precisely controlled dc voltage is made available from the voltage divider for the Modulator module carrier frequency.

Relays K5, K4, and K3 remain deenergized during normal operation to provide a black modulation frequency control level to the Modulator module. However, during the noise tests a gray Modulator output frequency is required and the relays become energized by a ground signal originated by the NOISE TEST flip-flop. This selects a different resistor for the voltage divider and provides a gray dc control for the Modulator module.

As mentioned earlier, the minus 20 volts supplied by one of five standards, is also fed to the oscillator control diode matrix. This matrix produces control levels from its 12 outputs which activate specific crystal-controlled oscillator switches to produce the precise reference frequency required for the standard selected. The correct switches are activated in the gray, black, and white oscillators, so that merely the applications of power to one or more of the oscillator circuits is required to obtain the correct gray, black, or white reference frequency from that oscillator. The particular frequency and the associated transistor switch that is selected are listed in the following table.

2. *White Insert.* This function inserts the selected white test frequency by electronic switching, into the vertical blanking interval, when the WHITE INSERT button is pressed.

Both the gray and black oscillators supply their outputs to respective transistor switching circuits that permit only one oscillator output to be supplied at any given time. Switch Q13 controls the gray oscillator output, and switch Q12 controls the black oscillator output. Either switch is deenergized by the position of relay K3, which biases either Q13 or Q12 to the "off" condition. The unbiased output is then amplified through FM driver subassembly A1 and supplied to the Modulator AFC module as the black or gray FM reference frequency.

TABLE 5—FREQUENCY STANDARD SELECTIONS

NOISE TEST FLIP-FLOP	*K3 K4 K5*	*Function Activated*	*STANDARD*				
			1 525 *LB MONO*	*2* 625 *LB MONO*	*3* 525 *LB COLOR*	*4* 525 *HIGH BAND*	*5* 625 *HIGH BAND*
RESET	Off	Black SW. Black Freq.	Q6 5.0 MHz	Q7 5.54 MHz	Q8 5.785 MHz	Q9 7.9 MHz	Q10 7.8 MHz
		White SW.* White Freq.	Q1 6.8 MHz	Q1 6.8 MHz	Q2 6.5 MHz	Q3 10 MHz	Q4 9.3 MHz
SET	On	Gray SW. Gray Freq.	Q14 6 MHz	Q14 6 MHz	Q14 6 MHz	Q15 9 MHz	Q16 8.5 MHz

* Activated only in E-E mode or in PLAY mode when white insert function is selected.

The white oscillator and crystal switches remain inoperative until energized through relay K1. With reception of a white insert signal from the Record Switch module, relay K1 connects operating power to the white oscillator and its associated switches.

White reference frequency is injected into the FM path following the vertical sync interval by an electronic switching arrangement using diode bridges Z1/Z2 and Z3/Z4. Normally the bridges are biased so that FM is supplied through the electronic switch. However, when white insert is operated, the bias is reversed and the white reference frequency is supplied for short intervals instead of FM. The timing intervals of the reference switch and FM switch are shown in the timing diagram, figure 27, which shows that the reference switch permits 37-microsecond pulses to pass during a 250-microsecond interval of vertical blanking.

A white insert command from the Record Switch module actuates relay K1 which energizes the white oscillator and enables diode gate CR33. Simultaneously, relay K1 allows the 9H pulses supplied from the Sync Logic module to trigger the 250-microsecond interval gate multivibrator (Q48, Q49). As shown in the timing diagram, the positive-going trailing edge of the 9H pulse triggers the interval gate multivibrator which provides a negative level of 250-microseconds duration to the diode gate (CR39, CR40).

Diodes CR39 and CR40 form a negative-input AND gate. The diode gate remains enabled for the 250-microsecond interval of the negative level. During this time a series of sync pulses supplied from the Modulator AFC module and passing through gate CR33 have been continuously triggering the 12-microsecond delay multivibrator (Q46, Q47). This multivibrator effectively delays the trailing edge of sync by 12 microseconds and is constantly supplying delayed trigger pulses to the diode gate at a horizontal rate.

The diode gate is enabled for 250 microseconds, therefore only a limited number of delayed Sync pulses pass through the gate. Those that pass trigger the white insert multivibrator (Q50, Q51) which supplies an equal number of 37-microsecond pulses. These pulses are split in phase through Q52, the opposite polarities are amplified through Q54 and Q55 and applied at opposite ends of the quad diodes using Z1 and Z2. This is the white insert diode bridge that functions as the reference switch.

The white oscillator output frequency is supplied from Q5 to the input of quad diodes Z1 and Z2. As the 37-microsecond pulses are supplied to the quad diodes, they forward bias the diodes and permit the white oscillator output to pass through the diodes. Thus during vertical intervals, white frequencies are supplied to the input of feedback amplifier Q44 and Q45.

The 37-microsecond pulses supplied from the white insert multivibrator are supplied to two phase splitters simultaneously. One output is fed to phase splitter Q52 (as described previously), while the second output is fed to Q53. The signal is also split through Q53, the opposite polarities are amplified through Q56 and Q57, and these outputs are applied at opposite ends of the quad diode bridge using Z3 and Z4. This is the FM diode bridge and functions as the FM switch.

Tape FM is supplied from the FM Equalizer module during playback operation. During E-E mode, E-E FM is supplied from the Record Switch module and relay K2 is activated by the E-E control signal from the Modulator AFC module. Thus, in either mode FM signals are supplied to the input of the Equalizer module.

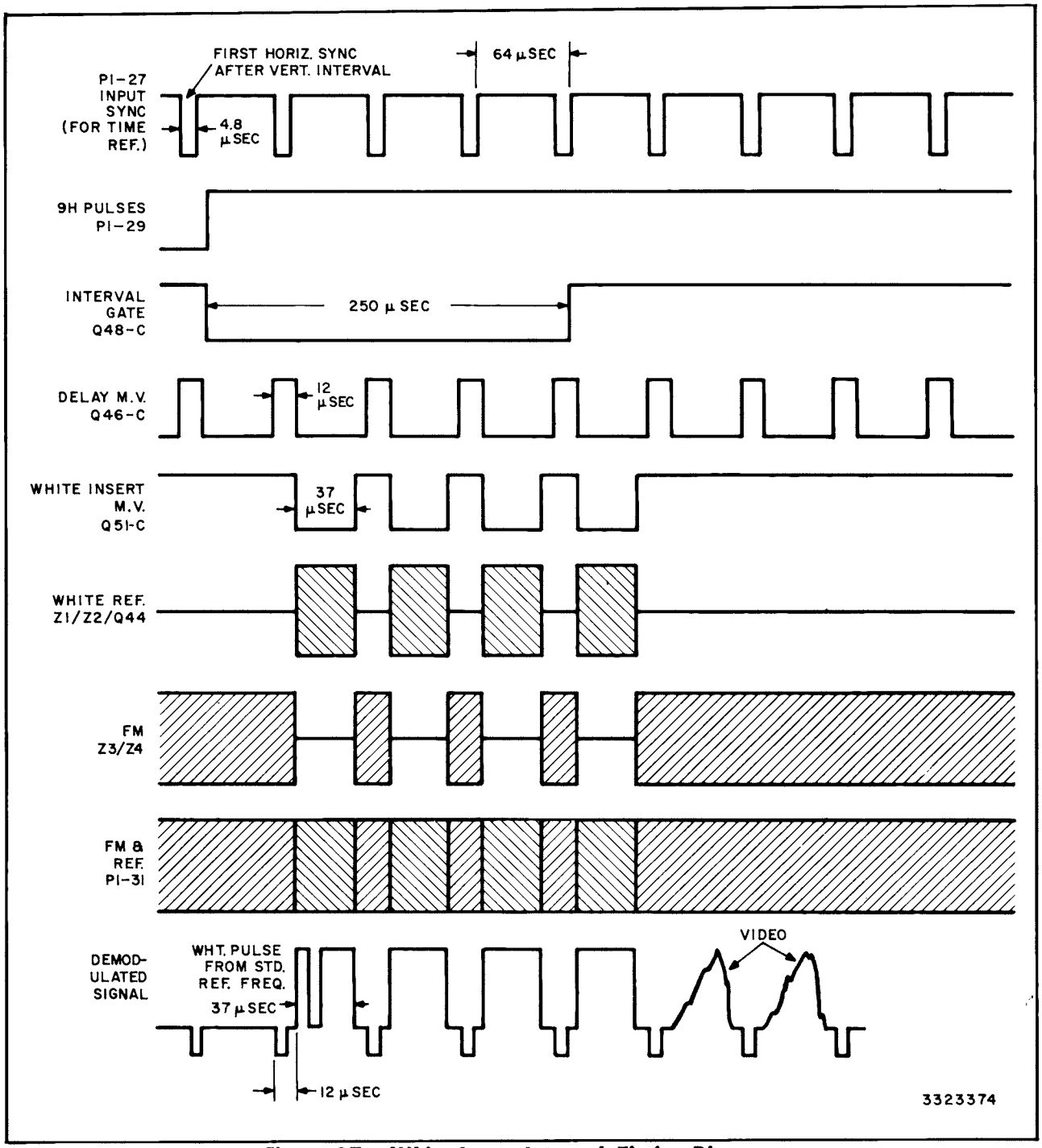


Figure 27—White Insert Interval, Timing Diagram

Polarities of the white insert gating signals supplied from the 37-microsecond multivibrator are arranged on both diode bridges so that one bridge is forward biased while the opposite bridge is simultaneously reverse biased. Thus, the FM diode bridge is forward biased except during the time of white insert. This permits FM to pass at all times except immediately following the vertical sync interval, at which time the white insert diode bridge becomes forward biased and allows the white frequency to pass.

The combined FM with white frequency which is inserted following the vertical interval are amplified through feedback amplifier Q44 and Q45. Unity gain amplification takes place in the output amplifier (Q58, Q59) to supply an output of 0.5 volt peak-to-peak to the FM Equalizer module.

3. *Test Control.* Provides control of relays K3, K4 and K5 when the machine is placed in the noise test mode. This is accomplished by pressing the push-button on the front panel, thus "setting" the noise test flip-flop and energizing relay K6. Energizing relay K6 places ground potential on relays K3-K5 which activates these relays. When relay K3 is activated, one of its contact arms supplies power to the gray oscillator switches and to the gray oscillator. The off bias previously mentioned, prohibits Q12 from functioning, therefore only gray frequencies are permitted to pass to the Modulator AFC module.

Also, in the test mode, white insert pulses can not be supplied to the reference switch.

A secondary contact of relay K6 supplies a ground potential to the TEST indicator on the RECORD panel and also to the Video Input module, where it disables the standard selection relays in the pre-emphasis network.

The noise test flip-flop is reset by activating the unlatch bus, which changes the state of Q38, Q39. Unlatch can be accomplished by pressing the stop button.

Gray Frequency Generator

The gray frequency generator consists of an oscillator (Q17) and three quartz crystals (Y10, Y11, Y12). Each crystal is associated with a transistor switch (Q14, Q15, Q16, respectively) which activates one of the crystals on command in a manner described below. Refer to figure 28.

The emitters of the three switching transistors are connected to a common bus which is bypassed to ground by capacitor C34. This bus is held at a nearly constant dc level of minus 0.45 volt by resistor network R79 and R80. The bases of the three switching transistors receive their input control signals from the diode matrix, and are biased by respective 11K-resistors R73, R75, and R77 which are connected to the plus 20-volt supply.

In the absence of a negative control signal from the diode matrix, the transistors are cut off by the positive level base bias. This produces an open circuit for the series circuit between the oscillator, crystal, and ac-ground through the switching transistor and capacitor C34.

To activate a crystal, the base of the associated transistor switch is driven negative by the negative level supplied from the diode matrix, which saturates the transistor switch and connects one side of the crystal to ground through capacitor C34. The opposite side of the crystal is connected to a common bus with all other crystals in that generator, and are all coupled through capacitor C35 to the base of oscillator Q17.

A Colpitts configuration is used for the oscillator circuit, with the collector of Q17 connected to ac ground. The selected crystal, which represents the resonant circuit in the oscillator is effectively connected between the base and collector of Q17 because of the saturated condition of its grounded switching transistor. Oscillation is sustained by feedback caused by the connection of the emitter to the capacitive voltage divider using C37 and C38.

Diode clipper CR20/CR21 limits the base voltage swing so that the output level becomes independent of transistor characteristics. Bias resistors R81 and R82, with emitter resistor R83 establish the dc conditions in the oscillator. The oscillator output is coupled through capacitor C40.

Power for the gray frequency generator is supplied only when the NOISE test mode has been selected by the NOISE TEST switch on the front panel. Refer to Table 5 for the frequency obtained for each operating standard.

Black Frequency Generator

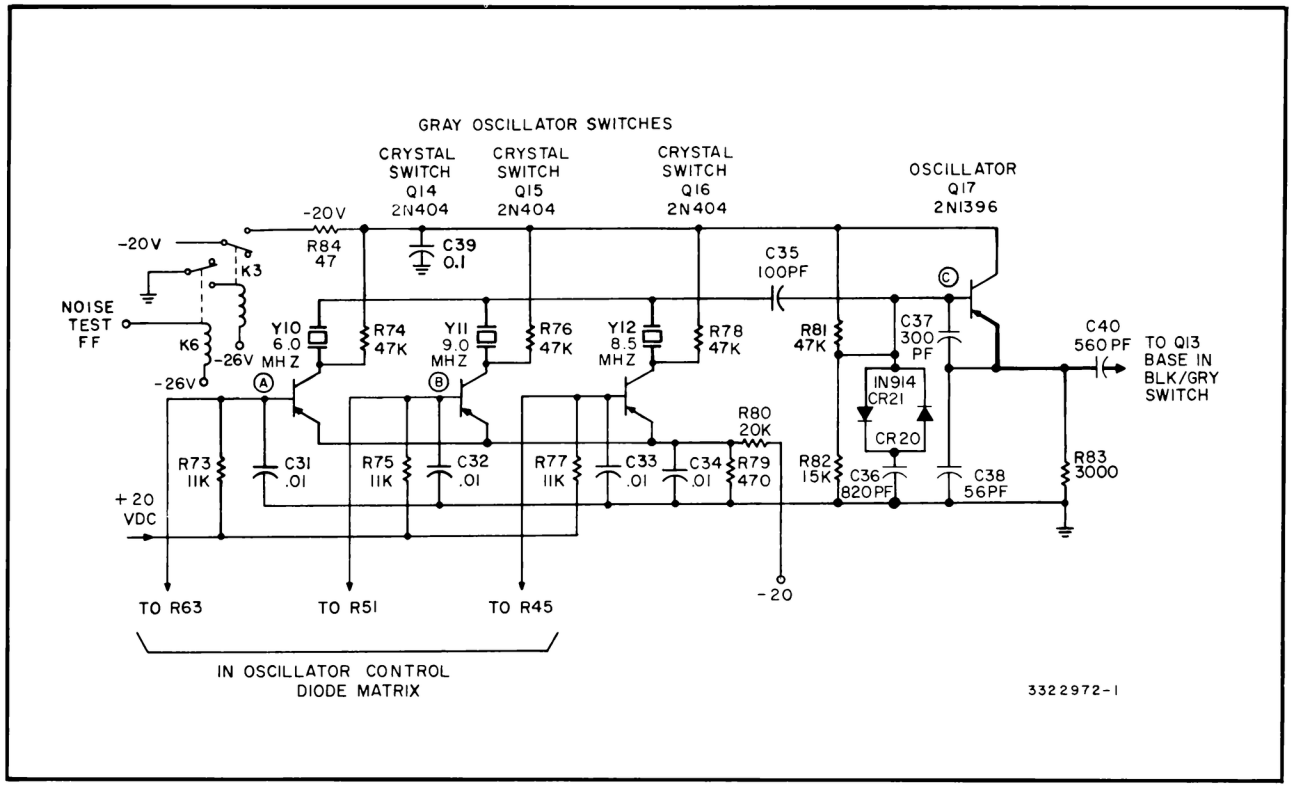
This generator supplies the black reference frequencies used in the Modulator AFC module to stabilize the Modulator module FM signal. The black frequency generator functions closely similar to the gray frequency generator except that five oscillator output frequencies can be obtained instead of three. Refer to figure 29.

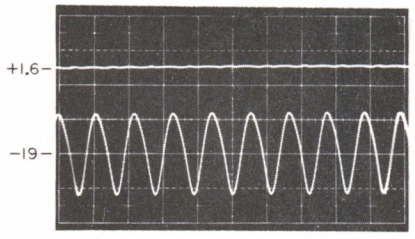
The basic functions of both generators are similar, therefore reference may be made to the description provided above for the gray frequency generator. The specific line standard, transistor, and frequency for the black oscillator frequencies are listed in Table 5.

White Frequency Generator

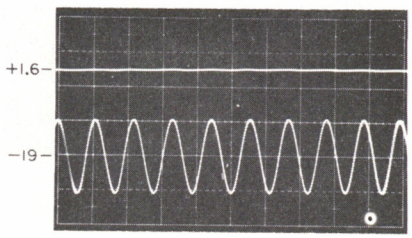
This generator contains four switch-controlled crystals that control the frequency of the white oscillator (Q5). The generator operates similarly to the gray and black frequency generators. The circuit is described previously for the gray frequency generator and reference should be made to that description. Refer to figure 30.

The seletced white reference frequency is supplied to the white insert quad diode bridge and may be

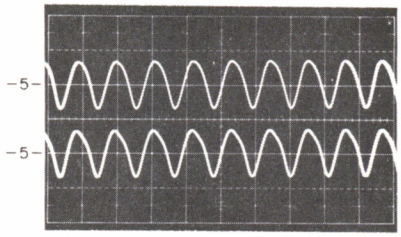




A. Top: Q14 base
Bottom: Q14 collector
Both: .2 v/cm, .1 μs/cm
Higband Standards



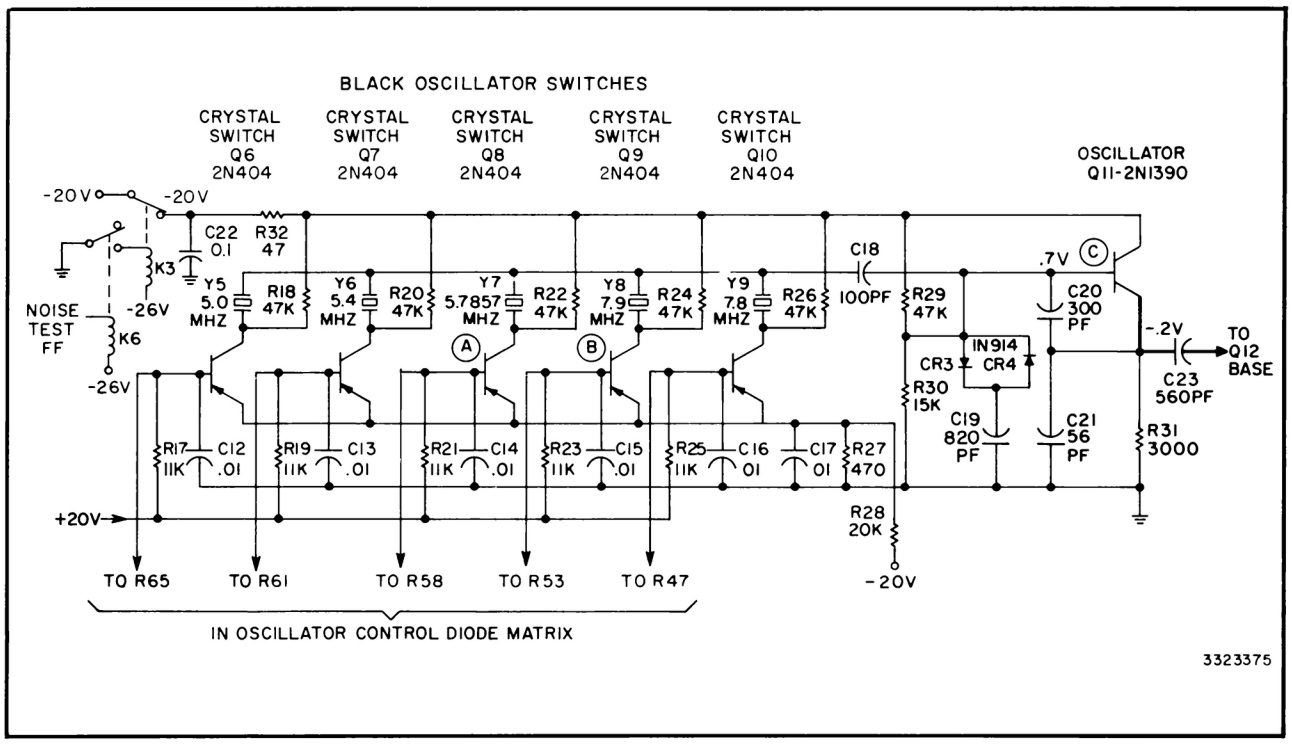
B. Top: Q15 base
Bottom: Q15 collector
Both: 2 v/cm, .1 μs/cm
Highband Color Standards

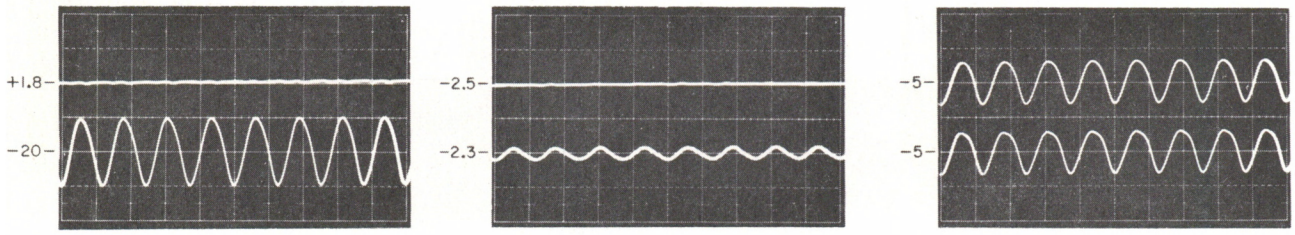


C. Top: Q17 base
Bottom: Q17 emitter
Both: 1 v/cm, .1 μs/cm
Highband Standards

All waveforms in E-E mode. TEST SELECT on NOISE position.

Figure 28—Gray Frequency Generator, Schematic Diagram and Typical Waveforms





A. Top: Q8 base
Bottom: Q8 collector
Both: .2 v/cm, .1 μs/cm
Highband Standards

B. Top: Q9 base
Bottom: Q9 collector
Both: .05 v/cm, .1 μs/cm
Highband Standards

C. Top: Q11 base
Bottom: Q11 emitter
Both: 1 v/cm, .1 μs/cm
Highband Standards

All waveforms in E-E mode.

Figure 29—Black Frequency Generator, Schematic Diagram and Typical Waveforms

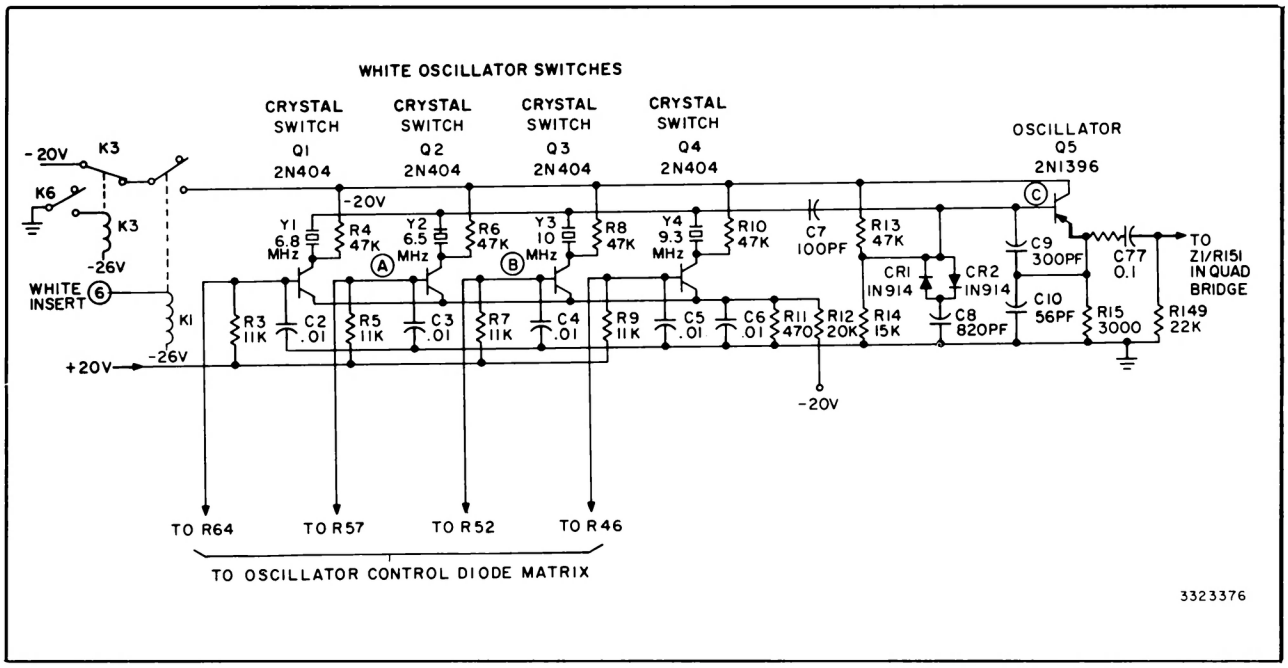
inserted in place of the FM signal during the vertical interval (described previously). Operating power for the white frequency generator is obtained when the WHITE INSERT pushbutton switch on the Record Switch module is depressed. Relay K1 is then energized and the black/white oscillator power (minus 20 volts) connects through the relay contacts to the collector circuits of the generator.

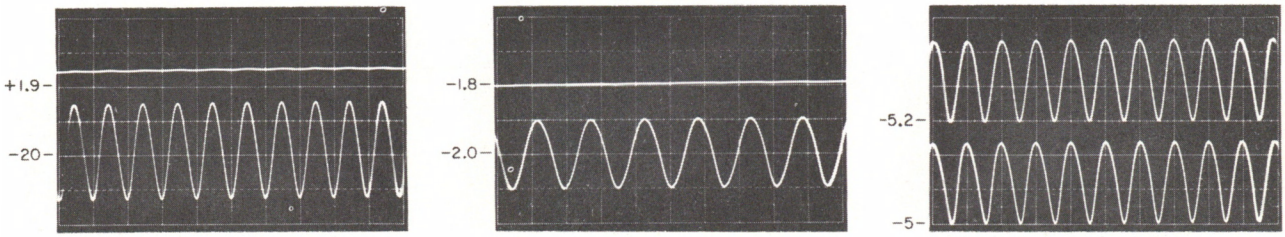
Frequencies supplied by the generator, together with associated transistor switches are listed with their appropriate standard selections in Table 5.

Oscillator Control Diode Matrix

Selection of a standard through the Standards Generator module supplies minus 20 volts to the selected input on the oscillator control diode matrix. The negative level forward biases the three diodes associated with the selected standard. Refer to figure 31.

Assume that the LB MONO switch on the Demodulator module and the 525 switch on the Vertical Advance module were selected. Minus 20 volts is then supplied through pin 13 of the FM Reference module from the Standards Generator, which forward biases diodes CR19, CR18, and CR16. Approxi-





A. Top: Q2 base
Bottom: Q2 collector
Both: .2 v/cm, .1 μs/cm
Highband Standards

B. Top: Q3 base
Bottom: Q3 collector
Both: .2 v/cm, .1 μs/cm

C. Top: Q5 base
Bottom: Q5 emitter
Both: .5 v/cm, .1 μs/cm
Highband Standards

All waveforms in E-E mode.

Figure 30—White Frequency Generator, Schematic Diagram and Typical Waveforms

mately minus 20 volts is now present at the junction of resistors R65/R68, R64/R67, and R63/R66, which results in an increased negative level on the bases of crystal-switching transistors Q6, Q1 and Q14 to cause them to saturate. At this time all remaining diodes in the matrix are not conducting, which reduces the negative level at the resistor junction and cuts off their related crystal-switching transistors.

With transistor Q6 saturated, the black frequency oscillator supplies an output of 5.0 MHz for blanking reference in the Modulator AFC module. Simultaneously, Q1 attempts to conduct and cause the white frequency oscillator to supply 6.8 MHz, while Q14 also attempts to conduct to connect the 6.0 MHz crystal to the gray oscillator, but these oscillators are inactivated because then collector supply voltage is removed. Depending on the conditions desired, the FM Reference module then supplies either the black or gray oscillator reference output (as selected through relay K3), and may inject 6.8 MHz for the white reference frequency during the white insert interval. When a different standard is selected with the Standards Generator, the minus 20-volt supply is removed from pin 13 and is applied to the pin associated with the new standard. This condition cuts off diodes CR19, CR18, and CR16, because of negative bias at their anodes from R68, R67 and R66, respectively, thus disabling transistors Q6, Q1, and Q14, while enabling the crystal-switching transistors controlling the newly selected standard.

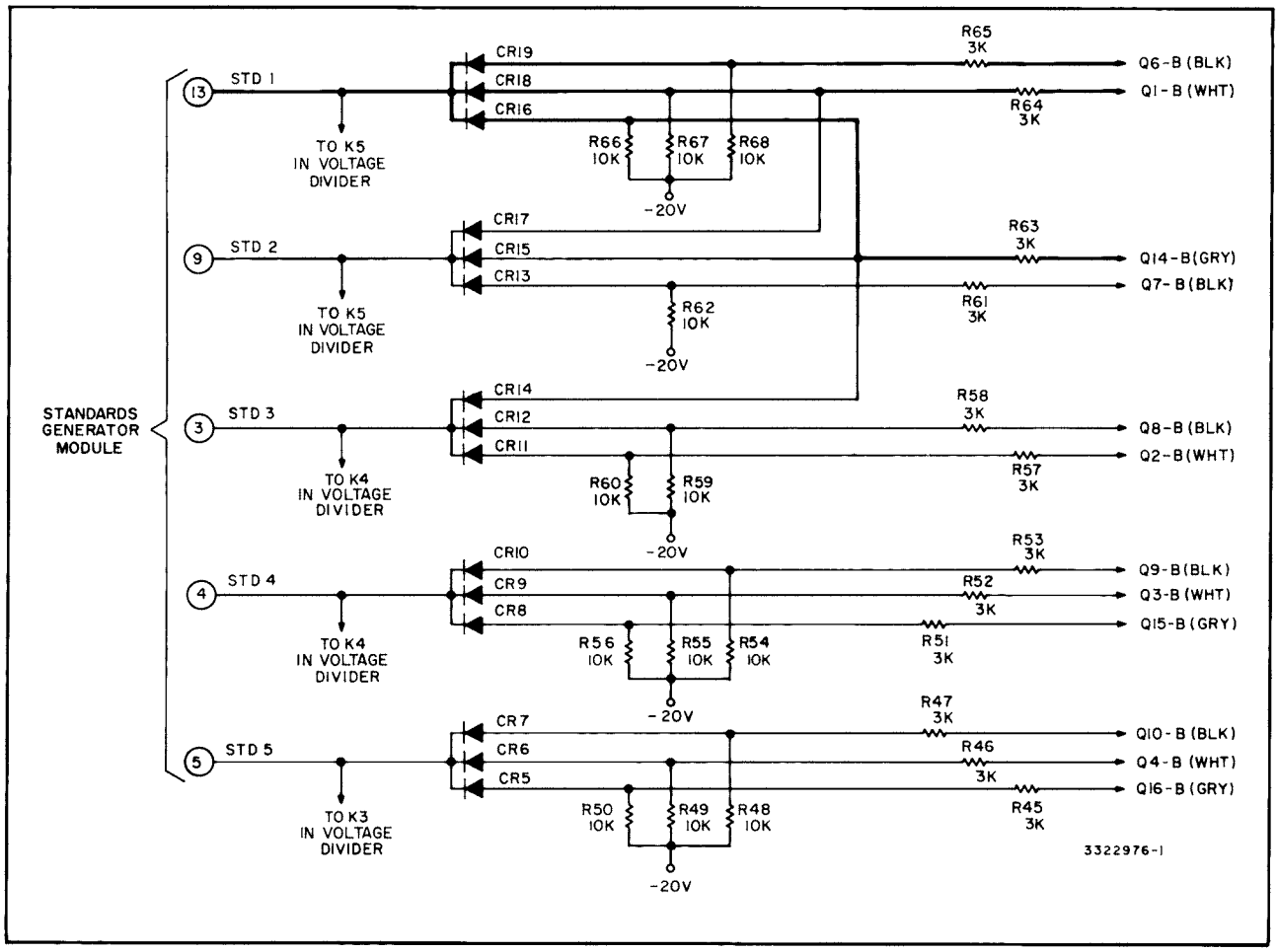


Figure 31—Oscillator Control Diode Matrix, Schematic Diagram

Black/Gray Switcher and Output

Outputs from the gray and black frequency oscillators are supplied to switching transistors Q13 and Q12, respectively. Only one transistor conducts, however, due to negative bias controlled by the contacts on relay K3. The operating switching transistor output is amplified through board A1 which supplies the black or gray reference frequency output. Refer to figure 32.

The voltage on the bases of Q12 and Q13 is set by voltage divider network R39 and R40 to approximately minus five volts. The emitter of Q12 is connected through resistor R36 to the normally-open contacts of relay K3. The emitter of Q13 is connected through resistor R44 to the normally-closed contacts of K3.

With relay K3 in the normal, deenergized condition, resistors R43 and R44 form another divider which sets the emitter potential of Q13 at minus 10 volts. Therefore Q13 is reverse-biased and the gray frequency does not pass through to the output. The black oscillator output is switched through transistor Q12, because the emitter of Q12 is connected to ground through resistor R35 and there is forward bias on the base of Q12.

Pressing the NOISE TEST switch on the front panel of the FM Reference module, sets the noise test flip-flop, energizes relay K6, energizes relay K3, and switches transistor Q12 off while switching Q13 on. This results in a gray frequency output to be supplied from the module for reference in the Modulator AFC module.

The collectors of Q12 and Q13 are connected together and the output of either conducting transistor is ac-coupled through capacitor C25 to input pin 2 of printed board subassembly A1. This board is mounted on the main terminal board and contains a series type output amplifier.

The collector of the first amplifier transistor on board A1 (Q1) is dc-connected to the base of its succeeding stage through a 12-volt Zener diode. The rf signal is ac-coupled from this collector/base connec-

tion through a capacitor (C1) which is in parallel with the Zener diode. The collector output of the second stage is combined with the emitter of the first amplifier stage to supply the output through pin 8 of the board. This is coupled through capacitor C30 and leaves the module through pin 17 to be supplied to the Modulator AFC module.

White Insert Control Multivibrators

Three multivibrators control white frequency insertion into the FM signal during tests. Inter-relation between these three multivibrators has been described previously showing their timing relationships. The following is a circuit description of the multivibrators to explain how their functions are accomplished.

1. Delay Multivibrator

The function of the delay multivibrator is to delay the white frequency reference signal for 12 microseconds, thus positioning the white lines (which are 37 microseconds in length) near the center of horizontal line intervals immediately following the vertical interval. This is accomplished by using the horizontal sync pulse to trigger the multivibrator. The time constant of the multivibrator is 12 microseconds, therefore the interval gate multivibrator is delayed by that amount. Refer to figure 33.

Transistors Q46 and Q47 form a monostable multivibrator with a time constant of 12 microseconds for its cycle period. During its quiescent state, transistor Q46 is held in saturation and Q47 is cut off. Plus 20 volts is applied to resistor R119 which forward-biases the base of transistor Q46 and causes it to conduct to saturation. The collector of Q46 then approaches ground level. Voltage divider R121/R122 causes the base of Q47 to be reverse-biased, and therefore held in cut-off condition. In addition, capacitor C64 becomes fully charged. Reception of a negative-going

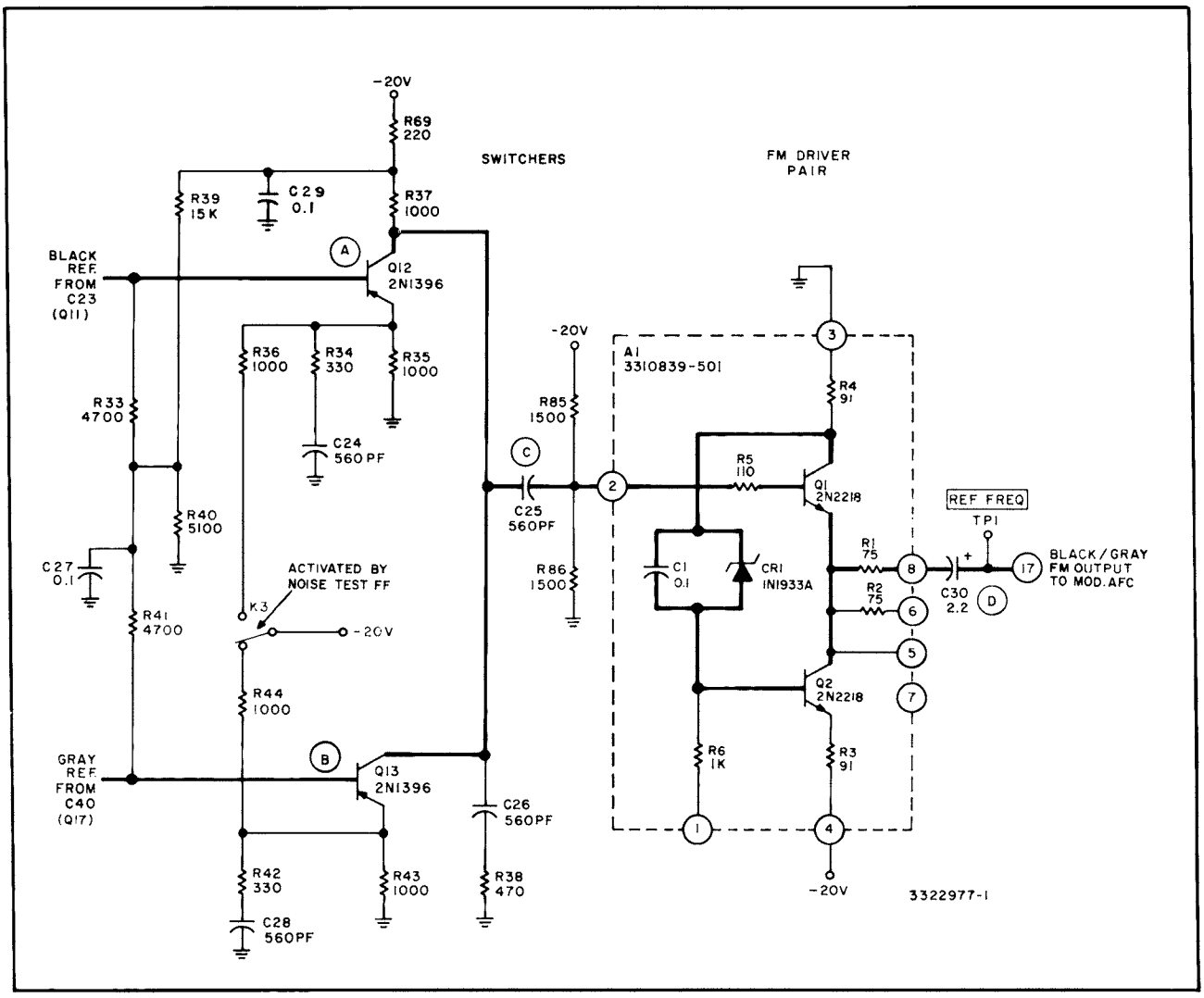
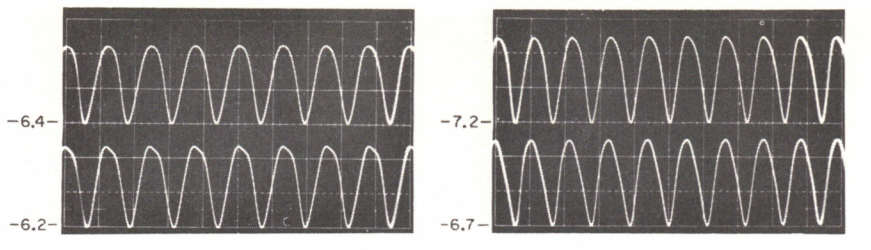
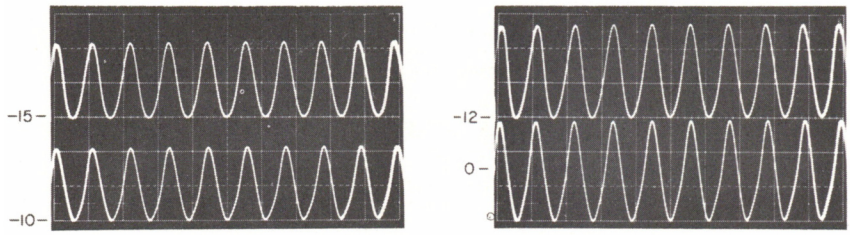


Figure 32—Black/Gray Switcher and Output, Schematic Diagram and Typical Waveforms



A. Top: Q12 base
Bottom: Q12 emitter
Both: .5 v/cm, .1 μs/cm

B. Top: Q13 base
Bottom: Q13 emitter
Both: .5 v/cm, .1 μs/cm



C. Top: Junction Q12/Q13 collectors
Bottom: A1 pin 2
Both: .5 v/cm, .1 μs/cm

D. Top: A1 pin 8
Bottom: TP1
Both: .2 v/cm, .1 μs/cm

All waveforms in E-E mode.

Figure 32—Black/Gray Switcher and Output, Schematic Diagram and Typical Waveforms (Continued)

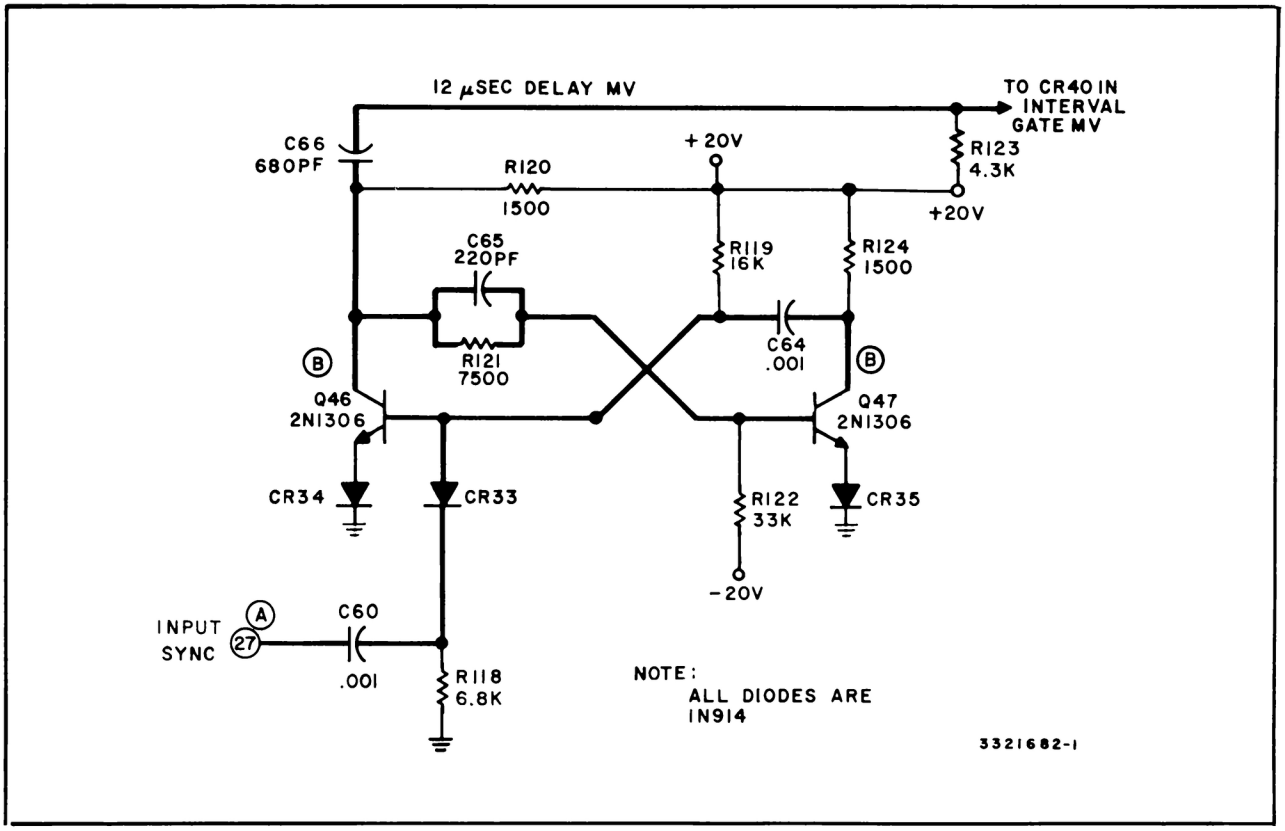
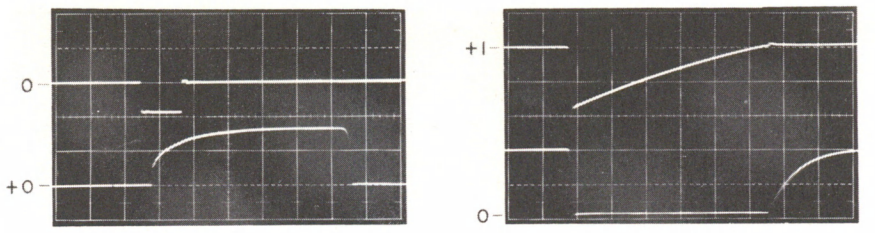


Figure 33—Delay Multivibrator, Schematic Diagram and Typical Waveforms



A. Top: P1 pin 27, 5 v/cm
Bottom: Q46 collector, 10 v/cm
Both: 2 μs/cm

B. Top: Q46 base
Bottom: Q47 collector
Both: 10 v/cm, 2 μs/cm

All waveforms in E-E mode.

Figure 33—Delay Multivibrator, Schematic Diagram and Typical Waveforms (Continued)

back porch clamp pulse reverses the condition and causes a positive pulse to be supplied from the collector of Q46.

Sync is supplied from the Modulator AFC module and is fed into the FM Reference module through pin 27. This pulse is coupled through capacitor C60 and forward-biased diode CR33 to cause the base of Q46 to become more negative. Transistor Q46 now cuts off and its collector rises toward plus 20 volts.

Cutting off transistor Q46 allows its collector to go positive because the voltage drop across resistor R120 decreases. The positive-going transition at Q46 collector is coupled through capacitor C65 to the base of Q47 and causes it to saturate. When Q47 saturates, its collector goes to ground and the resulting negative signal is coupled through C64 to the base of Q46, tending to cause Q46 to cut off more rapidly. Capacitor C64 now charges through resistor R119, and 12 microseconds later is charged sufficiently positive to turn on Q46 again and return the multivibrator to its quiescent condition. Diodes CR34 and CR35 in series with the transistor emitters disconnect the transistor from ground during cut-off conditions to avoid a high base-emitter reverse bias.

Diode CR33 is used as a gate which controls the passage of back porch pulses, depending on the presence of white oscillator power. Minus 20 volts for white oscillator power is supplied through the contacts of relay K1 whenever the WHITE INSERT button is pressed. The resultant current through resistor R108 biases diode CR33 "on" during these modes.

At other times (i.e. PLAY *without* white insert) the white oscillator power is blocked by relay K1, and diode CR33 is biased off by positive current from the plus 20-volt bus through resistor R109. The latter condition prevents back porch pulses from triggering delay multivibrator Q46/Q47, and thus stops the switching process in the fm and reference switches that are formed by diode bridges Z1/Z2 and Z3/Z4.

A positive output pulse having 12 microseconds width (as determined by time constant network R119/C64) is differentiated through capacitor C66, and applied to the anode of diode CR40. The diode is part of the negative AND gate using diodes CR40 and CR39 (further described later).

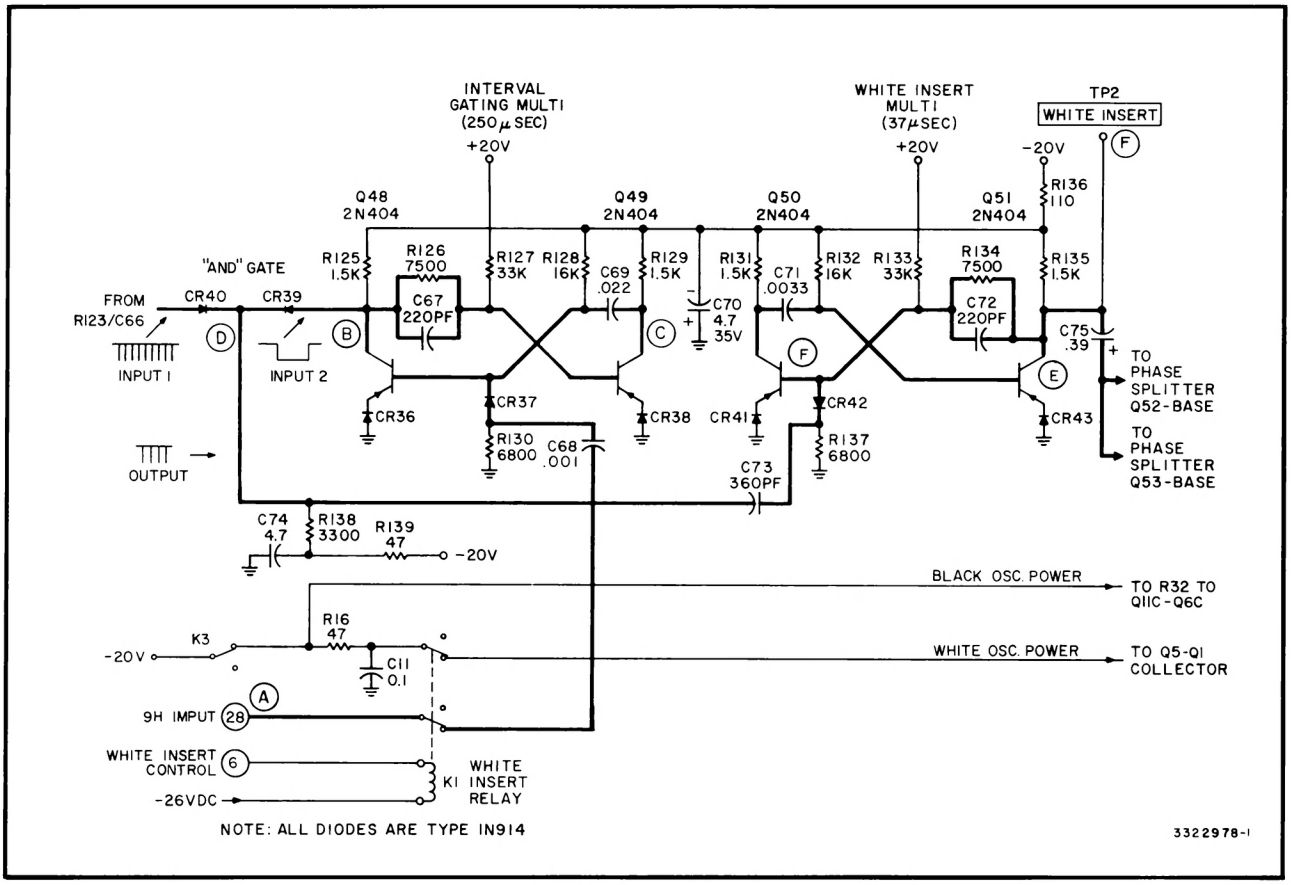
2. *Interval Gate and White Insert Multivibrators*

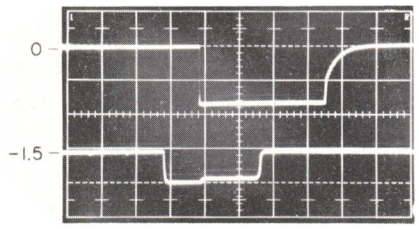
The interval gate multivibrator is a monostable type using transistors Q48 and Q49. Its operation is similar to that of the delay multivibrator (Q46/Q47) except that the minus 20 volts applied to resistor R128 forward-biases the base of Q48 (PNP type) and holds it saturated. Refer to figures 27 and 34.

A white insert control is supplied from the Record Switch module. This closes relay K1 and permits 9H pulses from the Sync Logic module to pass through the relay contacts, couple through capacitor C68 and be applied to the anode of diode CR37.

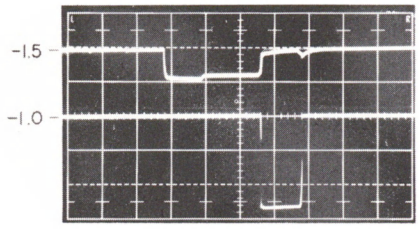
The trailing edges of the 9H pulses are positive going, and occur immediately after the equalizing pulses following vertical sync. These forward-bias diode CR37 and cause transistor Q48 to cut off. The multivibrator now changes state and remains thus for 250 microseconds, as determined by the time constant network using capacitor C69 and resistor R128. During this time the voltage on the collector of Q48 falls to minus 17 volts which provides a negative level on the anode of diode CR39, to reverse-bias the diode.

Diodes CR40 and CR39 with resistor R138 and capacitor C74 form a negative input AND gate.

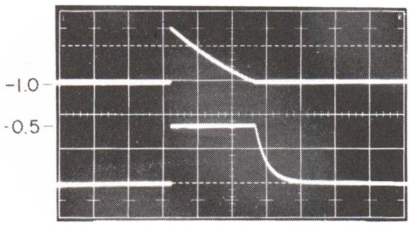




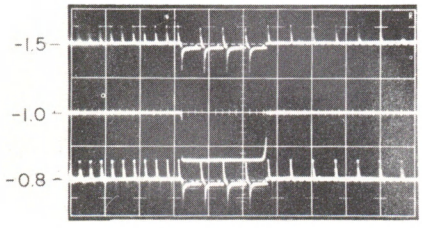
A. Top: Ref. Gen., Vert.
Bottom: P1 pin 28
Both: 5 v/cm, 0.2 ms/cm



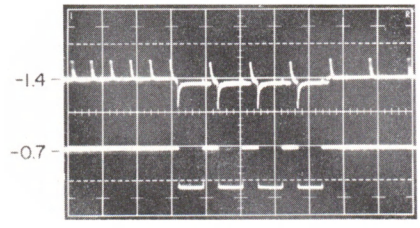
B. Top: P1 pin 28
Bottom: Q48 collector
Both: 5 v/cm, 0.2 ms/cm
Press White Insert Button



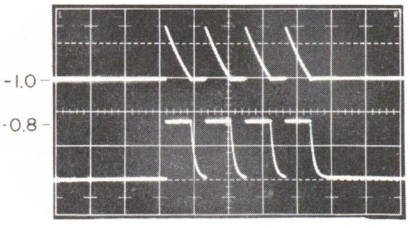
C. Top: Q48 base
Bottom: Q49 collector
Both: 10 v/cm, 0.1 ms/cm
Press White Insert Button



D. Top: CR39/CR40 cathode
Middle: CR39 anode
Bottom: CR40 anode
All: 10 v/cm, 0.1 ms/cm
Press White Insert Button



E. Top: CR39/CR40 cathode
Bottom: Q51 collector
Both: 10 v/cm, 50 μs/cm
Press White Insert Button



F. Top: Q51 base
Bottom: Q50 collector
Both: 10 v/cm, 50 μs/cm
Press White Insert Button

All waveforms in E-E mode.

Figure 34—Interval Gate and White Insert Multivibrator, Schematic Diagram and Typical Waveforms

When the anodes of diodes CR40 and CR39 have negative levels applied to them, the common junction (cathodes) of the diodes falls to a negative level. The negative signal is then coupled through capacitor C73 to change the state of the white insert multivibrator.

The negative AND gate can only supply a negative output when both of its inputs are negative. Thus, the gate becomes enabled for 250 microseconds by the negative level supplied from the interval gate multivibrator (Q48/Q49) and awaits negative pulses from the delay multivibrator (Q46/Q47), which are delayed for 12 microseconds from the start of horizontal sweep.

With each excursion of negative-going pulses from the delay multivibrator (during the 250-microsecond interval) the white insert multivibrator (Q50/Q51) is triggered to change state. This accomplished by forward-biasing diode CR42 which places a negative pulse on the base of Q50 and causes it to conduct.

Transistors Q50 and Q51 are part of the white insert multivibrator. This is a monostable type similar to the delay multivibrator and interval gating multivibrator. Capacitor C71 and resistor R132 form a time constant to cause the multivibrator to supply 37-microsecond negative-going pulses through capacitor C75. The pulses continue for the duration of time that the negative AND gate (CR40/CR39) supplies negative pulses as determined by the 250-microsecond interval multivibrator. Four or five pulses may be generated for each field. These pulses are supplied in parallel to phase splitters Q52 and Q53. During vertical intervals when the 250-microsecond pulse is not present on the anode of CR39, this diode is biased on and prevents passage of 12-microsecond trigger pulses.

Phase Splitters and Quad Diode Bridges

A phase splitter is used with each of the two quad diode bridges to insert the white reference frequency rf into the FM signal supplied from the tape or E-E circuits. The combined signals are then supplied to the amplifier and output circuits. Refer to figure 35.

Negative-going pulses in groups of four or five are supplied following the vertical interval, from the white insert multivibrator (Q50/Q51) to the parallel bases of Q52 and Q53. These two transistors split the phase of the 37-microsecond pulses from the multivbrator and fed separate diode quad switches through individual drivers.

The anode-cathode junctions of bridge Z1/Z2 are biased to minus 10 volts by voltage dividers R149/R151 and R153/R157. Positive-going pulses from the collector of Q52 are now coupled through C78 to the base of PNP type driver Q55. Until this time, transistors Q55 and Q54 were saturated, applying a ground level to the cathodes junction of Z1 and Z2, and a negative level (−20 volts) to the anodes junction of Z1 and Z2, to reverse bias the bridge. With reception of positive-going pulses, Q55 stops conducting, and allows minus 20 volts to be connected through resistor R152 to the cathodes junction of Z1 and Z2, thereby forward biasing one-half of the bridge.

Simultaneously, negative-going pulses from the phase splitter (Q52) are supplied from its emitter, coupled through capacitor C76 to cut off normally conducting NPN type driver Q54. The anodes junction of Z1 and Z2 are then connected to ground through resistor R150 and the entire quad diode bridge is forward biased.

White reference frequency rf supplied from the emitter of oscillator Q5 is coupled through capacitor C77 and applied to the input of Z1 on the quad diode bridge. When the bridge is forward biased, the white frequency rf passes through the bridge and is coupled through capacitor C81 in the amplifier and output circuits. At this time the opposite diode bridge using Z3 and Z4 is reverse biased and prevents tape FM or E-E FM from passing through.

The negative-going pulses supplied in parallel to the base of phase splitter Q53 have the opposite effect on the FM diode bridge (Z3/Z4). The collector of Q53 supplies positive-going pulses that saturate NPN type driver Q56. The collector of Q56 places a negative level (−20 volt) on the anodes junction of Z3 and Z4 thereby cutting off the diodes in this section of the bridge.

Negative-going pulses from the emitter of phase-splitter Q53 saturate PNP type driver Q57 and place a ground level on the cathodes junction of Z3 and Z4. Thus, the FM diode bridge is reverse biased at the same time that the white insert bridge is forward biased. After white frequency insertion is complete, the entire process is reversed and Z1/Z2 is cut off white Z3/Z4 is conducting to permit tape FM or E-E FM to pass while inhibiting the white reference rf from passing.

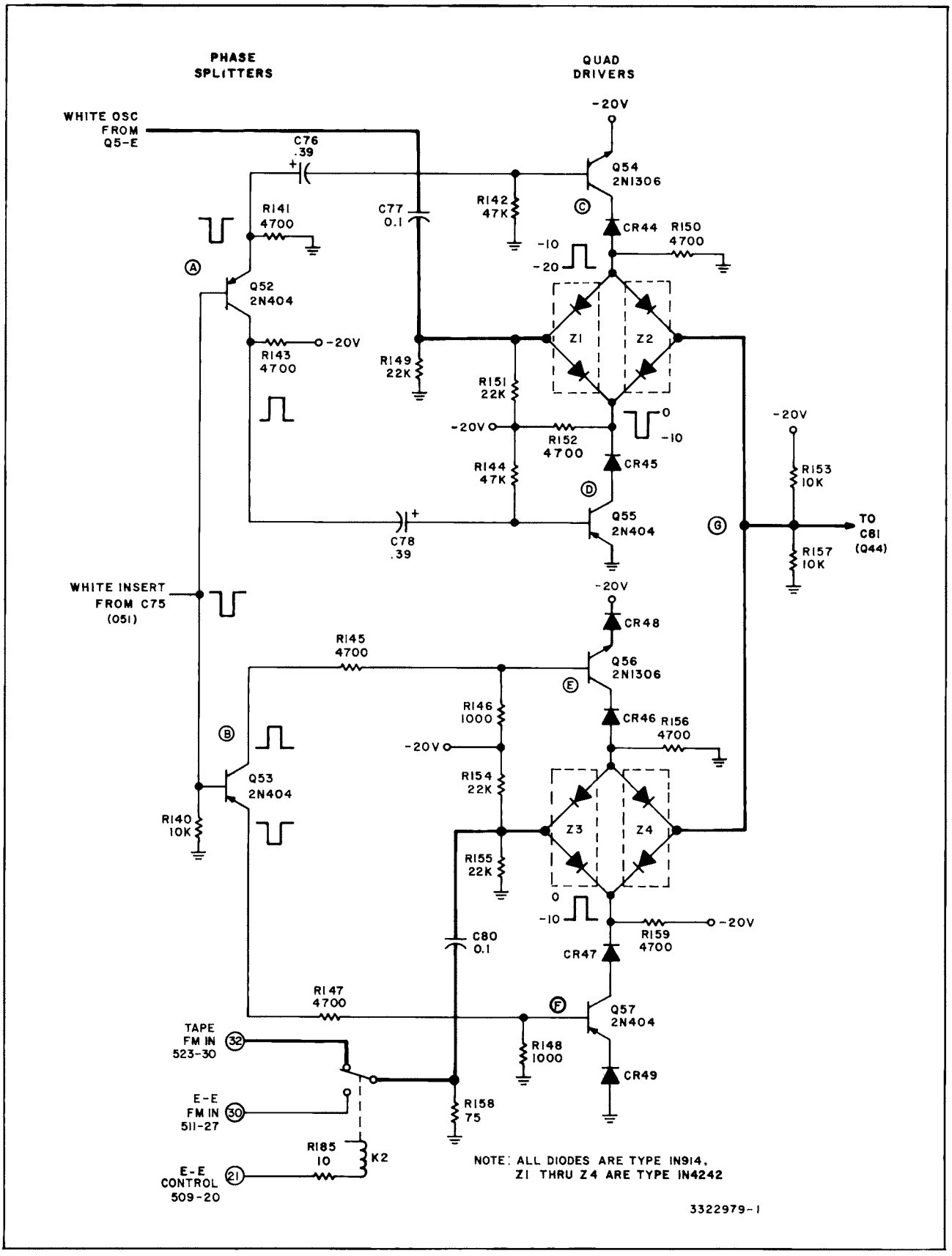
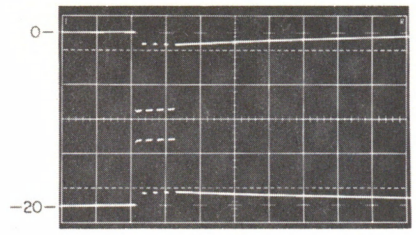
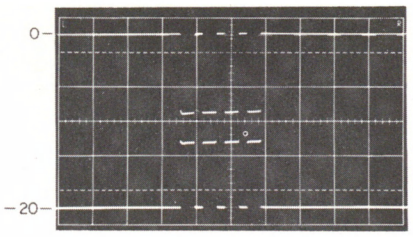


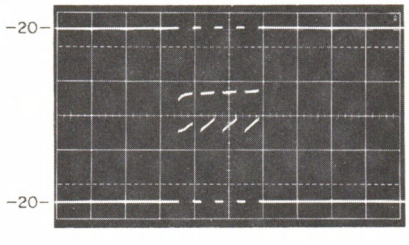
Figure 35—Phase Splitters and Quad Diode Bridges, Schematic Diagram and Typical Waveforms



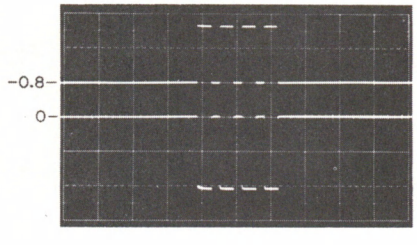
A. Top: Q52 emitter
Bottom: Q52 collector
Both: 5 v/cm, .2 ms/cm



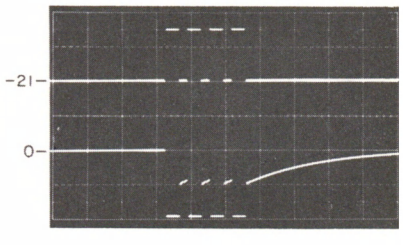
B. Top: Q53 emitter
Bottom: Q53 collector
Both: 5 v/cm, .1 ms/cm



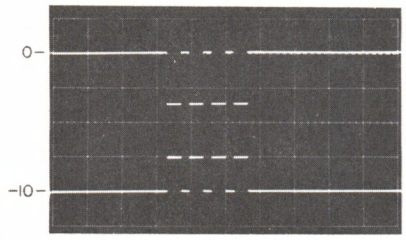
C. Top: Q54 base
Bottom: Q54 collector
Both: 5 v/cm, .1 ms/cm



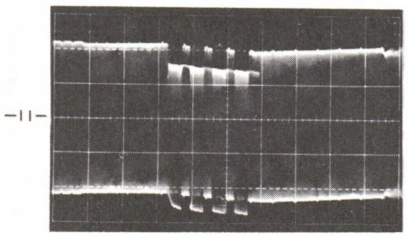
D. Top: Q55 base
Bottom: Q55 collector
Both: 5 v/cm, .1 ms/cm



E. Top: Q56 base, 1 v/cm
Bottom: Q56 collector, 10 v/cm
Both: .1 ms/cm



F. Top: Q57 base, 1 v/cm
Bottom: Q57 collector, 10 v/cm
Both: .1 ms/cm



G. Junction R153/R157
.05 v/cm, .1 ms/cm

All waveforms in E-E mode.

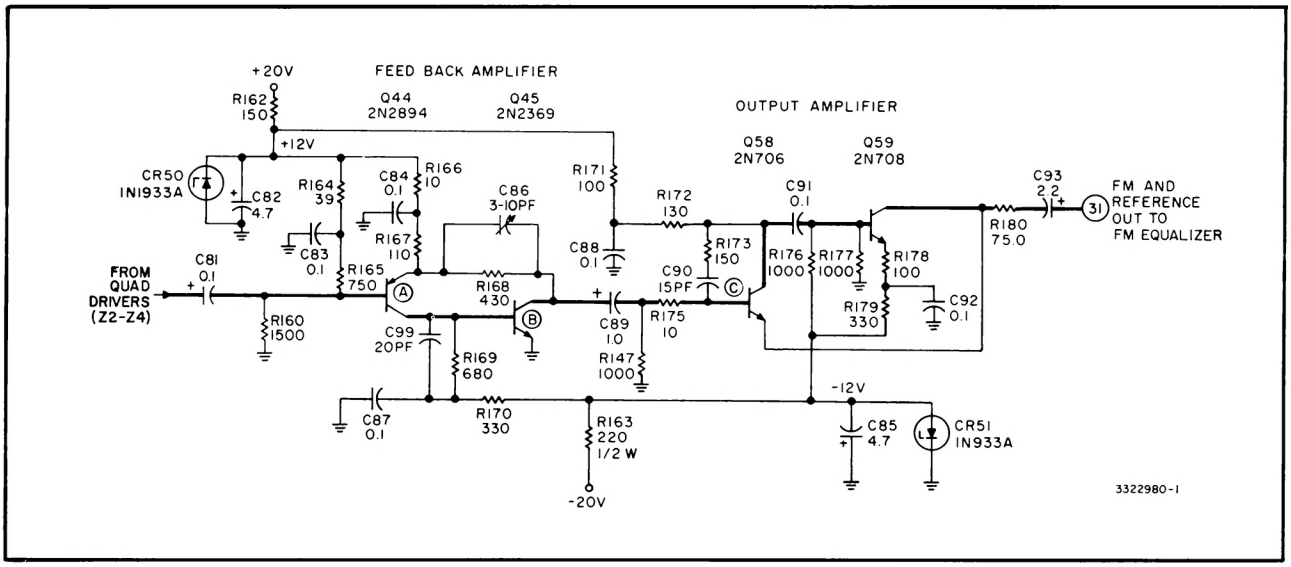
Figure 35—Phase Splitters and Quad Diode Bridges, Schematic Diagram and Typical Waveforms (Continued)

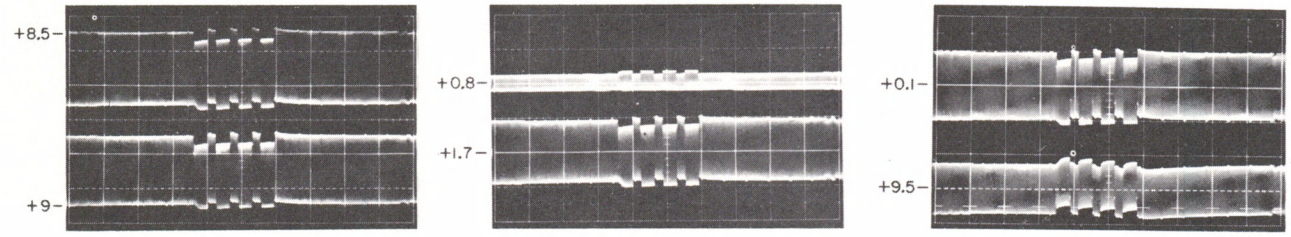
Amplifier and Output

The signal supplied from the quad drivers consists of tape FM or E-E FM with bursts of white reference frequency rf. This signal is amplified through the feedback voltage amplifier stage, isolated through the unity-gain output feedback amplifier and supplied from the module as the FM and reference frequency output. Refer to figure 36.

A parallel output from the two quad diode bridges is ac-coupled through capacitor C81 and applied to the base of Q44. Transistors Q44 and Q45 form a feedback amplifier that increases the voltage of the FM and white frequency reference signal. The collector of Q44 is coupled directly to the base of Q45 whose collector supplies a feedback signal through R168 and trimmer capacitor C86. The trimmer is adjusted for flat response. Resistors R168 and R167 are in the ratio of four-to-one, resulting in an overall gain of five.

Output from the feedback voltage amplifier is taken from the collector of Q45 and coupled through capacitor C89 and through parasitic suppressor resis-





A. Top: Q44 base
Bottom: Q44 emitter
Both: .1 v/cm, .1 ms/cm

B. Top: Q45 base, .05 v/cm
Bottom: Q45 collector, .5 v/cm
Both: .1 ms/cm

C. Top: Q58 base, .5 v/cm
Bottom: Q58 collector, .2 v/cm
Both: .1 ms/cm

All waveforms in E-E mode.

Figure 36—Amplifier and Output, Schematic Diagram and Typical Waveforms

tor R175, to the base of Q58. Transistors Q58 and Q59 are cascaded to supply a common output. Capacitor C91 couples the signal from the resistor of Q58 to the base of Q59. Resistor R172 provides a load for Q58. The collector output of Q59 is fed back to the emitter output of Q58 to provide 100 percent feedback and a gain of unity. Resistor R180 provides 75-ohm termination from the extremely low amplifier output impedance, and capacitor C93 couples the signal through pin 31 to the FM Equalizer module.

Frequency Control Voltage Divider

This voltage divider consists of a group of resistor networks that divide between plus 20 volts and minus 20 volts to provide a dc level for frequency control of the Modulator carrier. Selection of the resistor networks is accomplished through the Standards Generator, and black/gray selection from the NOISE TEST switch on the front panel of the FM Reference module. Refer to figure 37.

The Standards Generator provides five lines for Modulator module frequency control. The selected line is at minus 20 volts and all other lines are on open circuit. These lines are used only for Modulator frequency control as well as reference crystal selection, and are supplied to the resistor network in the FM Reference module. Selecting an operating standard allows minus 20 volts to proceed through the contacts of relays K3, K4, or K5 and through resistors in the network. The relay coils are controlled in parallel by the noise test relay K6.

Plus 20 volts is connected through resistor R183 which is common for all resistor networks. The junction point of the resistors in the network provides a dc level that is associated with the selected operating standard. This dc level is supplied to the Modulator module where it is eventually applied to voltage controlled oscillators that generate the FM carrier, thus controlling the Modulator carrier frequency.

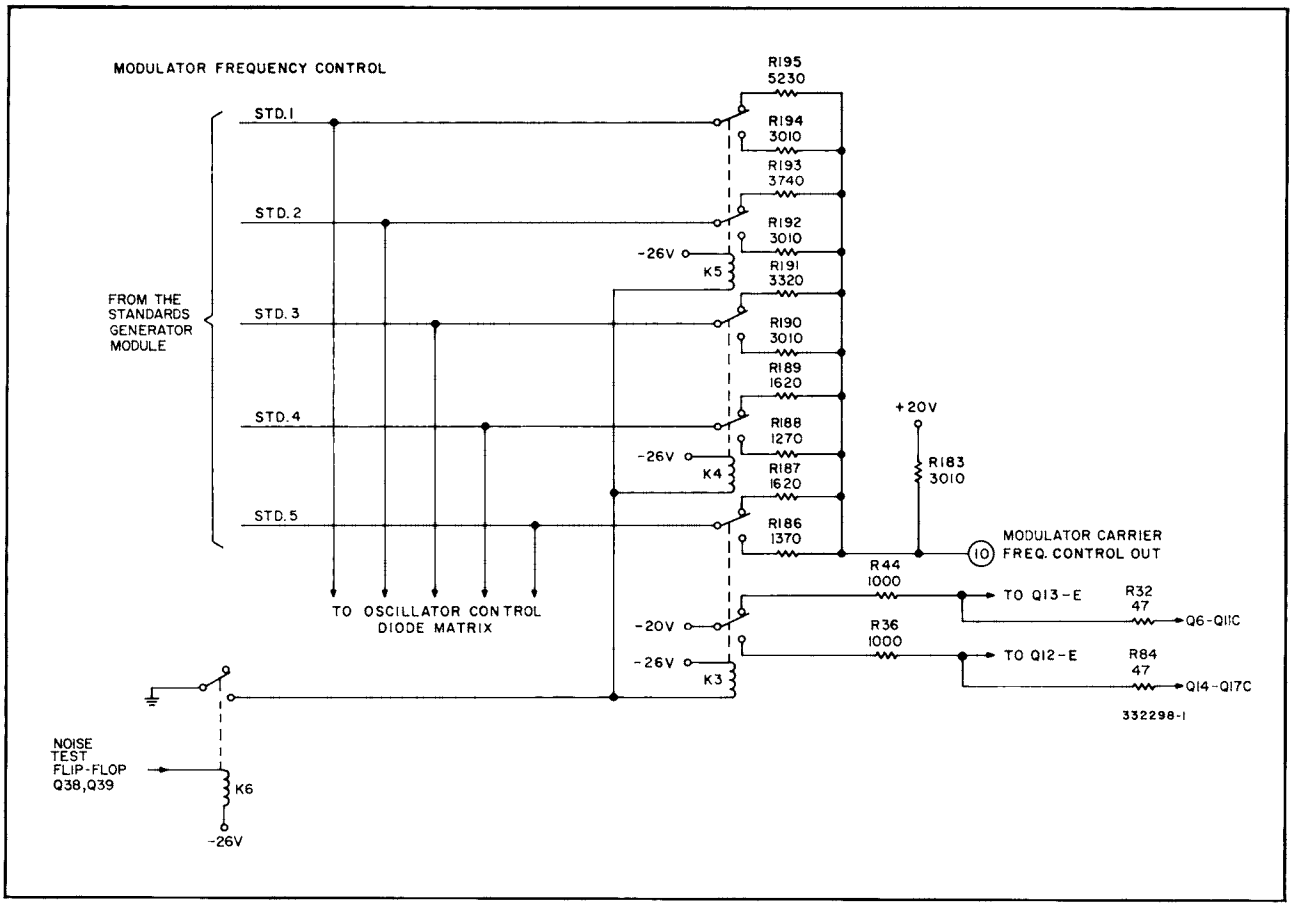


Figure 37—Frequency Control Voltage Divider, Schematic Diagram

Noise Test Flip-Flop

This circuit provides the necessary control level through relay K6 to energize relays K3, K4 and K5. In addition, it provides a level to light the TEST indicator on the RECORD panel and also disable the pre-emphasis relay in the Video Input module. Refer to figure 38.

Transistors Q38, Q39 form a bistable multivibrator. In its quiescent state, Q38 is conducting and Q39 is cut off. The base of Q39 is at +0.6 volts keeping the PNP transistor off, while the base of Q38 is at a negative potential keeping it saturated. Pressing the NOISE TEST pushbutton switch, S1, places +0.6 volts on the base of Q38. This causes Q38 to cut off and its collector potential falls toward −26 volts. This negative potential is coupled through diode CR23 to the base of Q39, causing it to saturate. With ground potential at the collector of Q39, relay K6 energizes. The flip-flop will remain in this state until reset by the unlatch bus pulse which turns Q38 back on.

One set of contacts on relay K6 provides a ground return for relays K3, K4 and K5 in the standards generator circuitry in this module. Another set of contacts on relay K6 also provides a ground potential to the pre-emphasis relays in the Video Input module, and to the TEST indicator on the RECORD panel during noise test. In the unenergized position, K6 supplies −26 volts to the pre-emphasis network.

The unlatch bus pulse is negative-going and is coupled through diode CR24 to the base of Q38 where it changes the state of the flip-flop. The −13 volt pulse causes C38 to conduct heavily which removes the −26 volts from the base of Q39. Thus, Q39 no longer is saturated, but cut off by the 0.6 volts on its base. Therefore, relay K6 is deenergized.

ADJUSTMENTS

The FM Reference module has been carefully adjusted at the factory and should not be disturbed. All internal adjustments in this module are set to close tolerances with special test equipment, and do not require further adjustment. All adjustment settings have been locked in place with red or blue sealing compound. If service is required, contact your RCA representative.

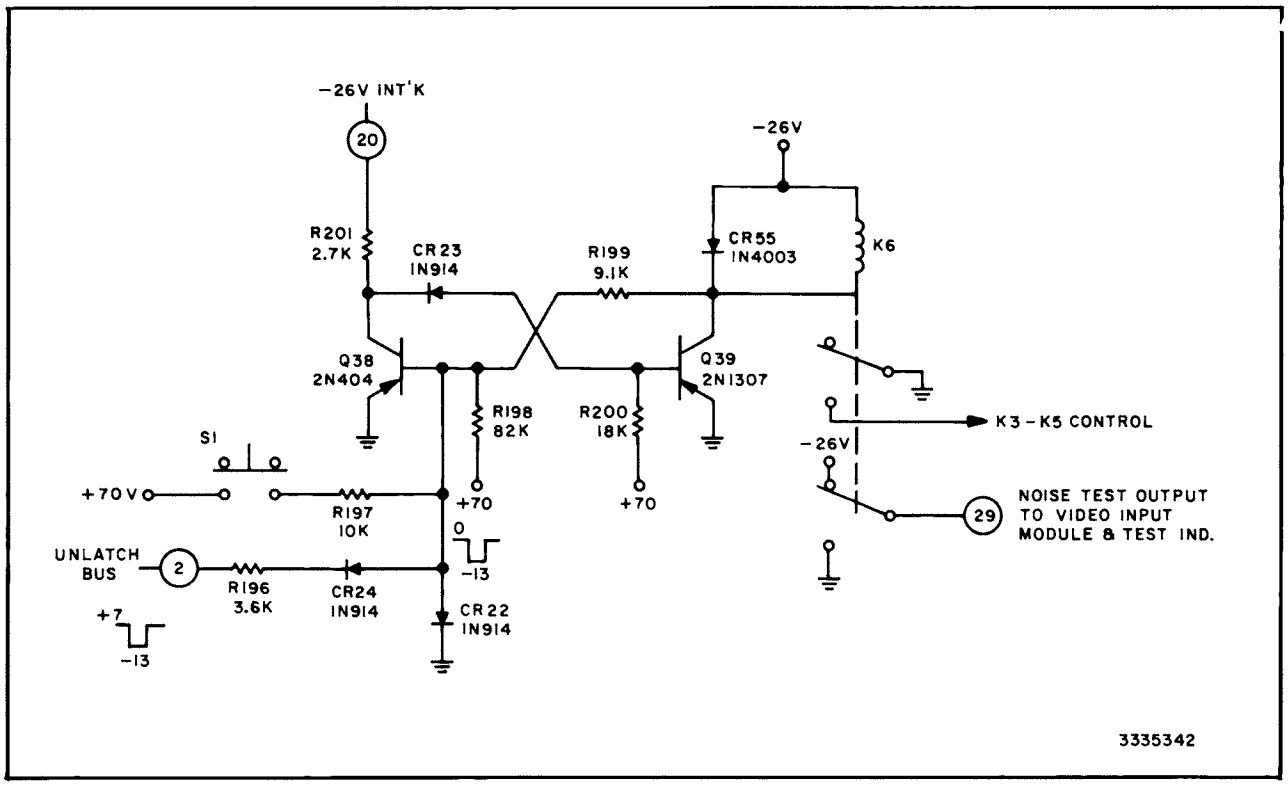


Figure 38—Noise Test Flip-Flop, Schematic Diagram and Typical Waveforms

RECORD SWITCH MODULE

CIRCUIT DESCRIPTION

General

The Record Switch module is activated during RECORD and RF COPY modes to equalize current flow through the quadrature heads by reducing low frequency current and increasing high frequency current. This is required to compensate for the head inductive characteristics. A splice switching circuit is included that functions during tape splice operations. Refer to the block diagram, figure 39.

During RECORD mode, the FM signal from the Modulator module is applied to emitter follower Q1. During RF COPY mode, the FM signal supplied to the machine is fed in through a jack on the machine connector panel and applied to the module via pin 19. After passing through the RF COPY control, the signal is applied to emitter follower Q2. During normal operation, relay K1 remains deenergized and the FM signal from transistor Q1 passes through the relay contacts.

After passing through relay K1, either the rf copy or FM record signal (depending on the condition of K1) is fed to two signal paths in parallel. One signal path is to feedback emitter follower Q3/Q4, which is the first stage of the record path. The other signal path is to emitter follower Q21 that supplies the selected signal to a line amplifier (Q22/Q23). The amplifier provide the output signal that check the electronic-to-electronic (E-E) signal path.

The output from the feedback emitter follower Q3/Q4 is supplied to a splice switching circuit which is activated by levels appearing at either pin 32 (record/setup) or at pin 27 (splice record control). In machines not having the electronic splice accessory, the level at pin 27 is floating, and therefore transistor Q20 determines the state of the splice switch. During RECORD mode, the level at pin 32 goes high (ground) and the splice switch becomes activated to allow the signal to pass to the base of emitter follower Q5 described below.

In machines equipped with the electronic splice accessory, the level at pin 27 becomes negative during normal operation, and again transistor Q20 determines the state of the splice switch. When electronic

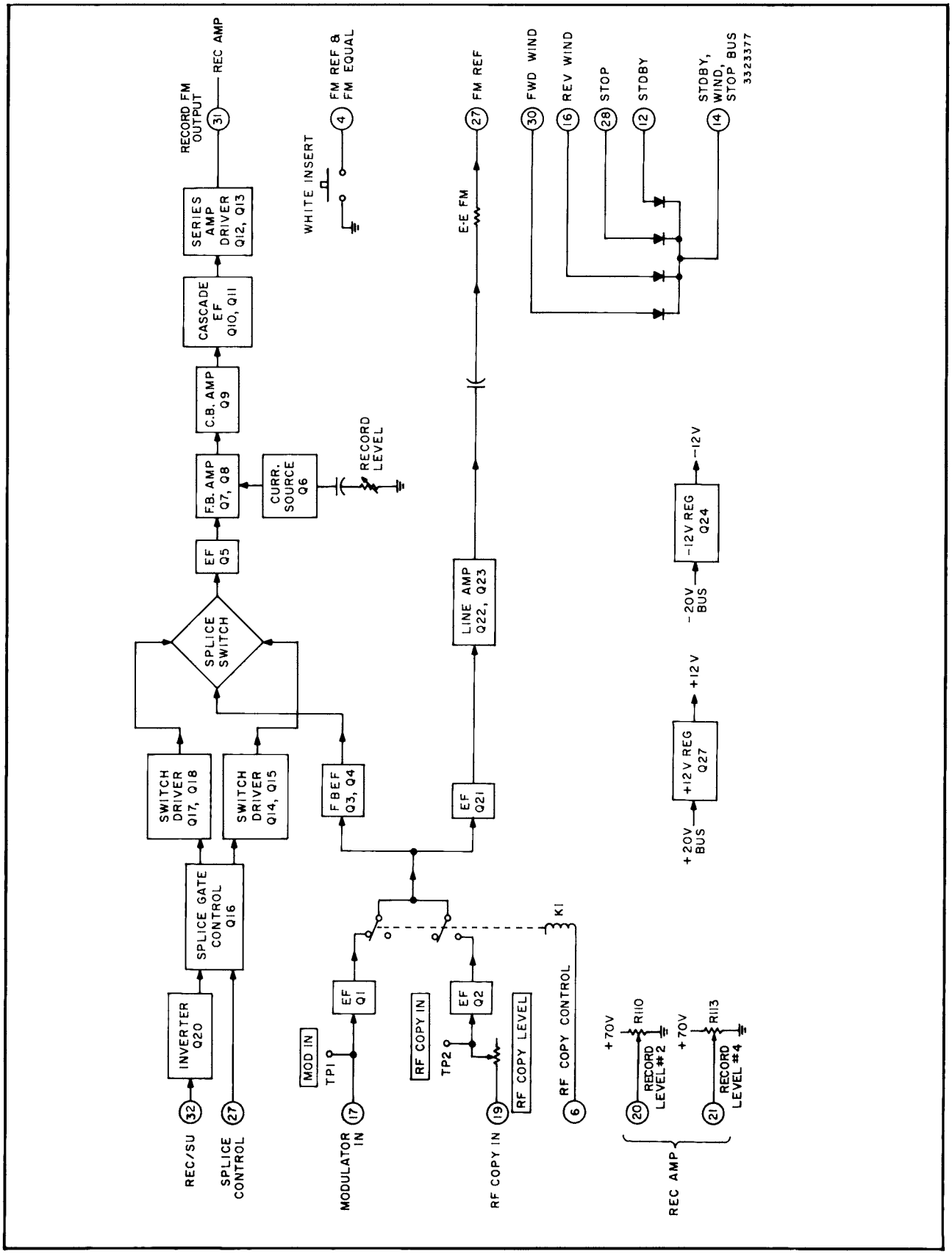


Figure 39—Record Switch Module, Block Diagram

splicing is required, and the machine is properly set for splice, the level at pin 27 goes high with the depressing of the PLAY button. This level then deactivates the splice control switch and transistor Q20 no longer controls the switch state. To accomplish a splice, the MASTER RECORD button is depressed causing the level at pin 32 to go high and holds the level at pin 27 high for one-half second (with tape speed at 15 inches-per-second), then goes negative. The negative-going level on pin 27 causes a very rapid reversal of the splice switch state and allows the FM signal to pass and be recorded on tape. (The splice function is fully described in IB-31872).

When the splice switch is activated, the FM signal is permitted to be supplied to emitter follower Q5. Output from Q5 is fed to feedback amplifier Q7/Q8 where equalization of the RECORD level through transistor Q6 is inserted into the FM signal. The resulting signal is amplified through transistor Q9 and cascaded through transistors Q10 and Q11 before being supplied to the line driver circuit.

Series amplifier Q12/Q13 furnishes the output FM signal to the Record Amplifier module which in turn drives the quadrature heads. Resistor R55 in conjunction with the amplifier impedance sending end, provides 75 ohms termination for the output line.

Record level controls for channel 2 and 4 are housed on the front panel of the Record Switch module. They have no affect on the circuitry in this module.

The WHITE INSERT switch is also located on the front panel of the Record Switch module and is used to activate the white insert circuitry in the FM Reference module and the FM Equalizer module.

A diode matrix that makes up the Standby, Wind and Stop bus is housed in the Record Switch module. The matrix is a four input OR gate. Any time one or more of the signals is high (ground) the Standby, Wind, Stop bus is activated.

Input Signals

Two separate inputs are supplied to the module, one is from the Modulator module, fed in through pin 17, and applied to the base of transistor Q1. See figure 40. This is the FM signal that is to be recorded. The other input to the module is rf copy supplied to the machine through a jack, fed in through pin 19 of the module connector, and applied to the base of transistor Q2 after attenuation with potentiometer R63 (RF COPY LEVEL) and resistor R62. Test points TP1 and TP2 permit monitoring the input signals with an oscilloscope.

The function of input transistors Q1 and Q2 are emitter followers with a silicon diode at their emitters to inhibit conduction through the transistor when its counterpart input is selected. Input selection is accomplished by the condition of relay K1. Under normal RECORD operating conditions, relay K1 is deenergized and the recording FM signal from transistor Q1 passes through the relay contacts. When the RF COPY mode is selected, relay K1 becomes energized by the rf copy control signal supplied through pin 6 to the relay coil. This causes the rf copy signal from transistor Q2 to pass through the relay contacts, while inhibiting the record FM signal.

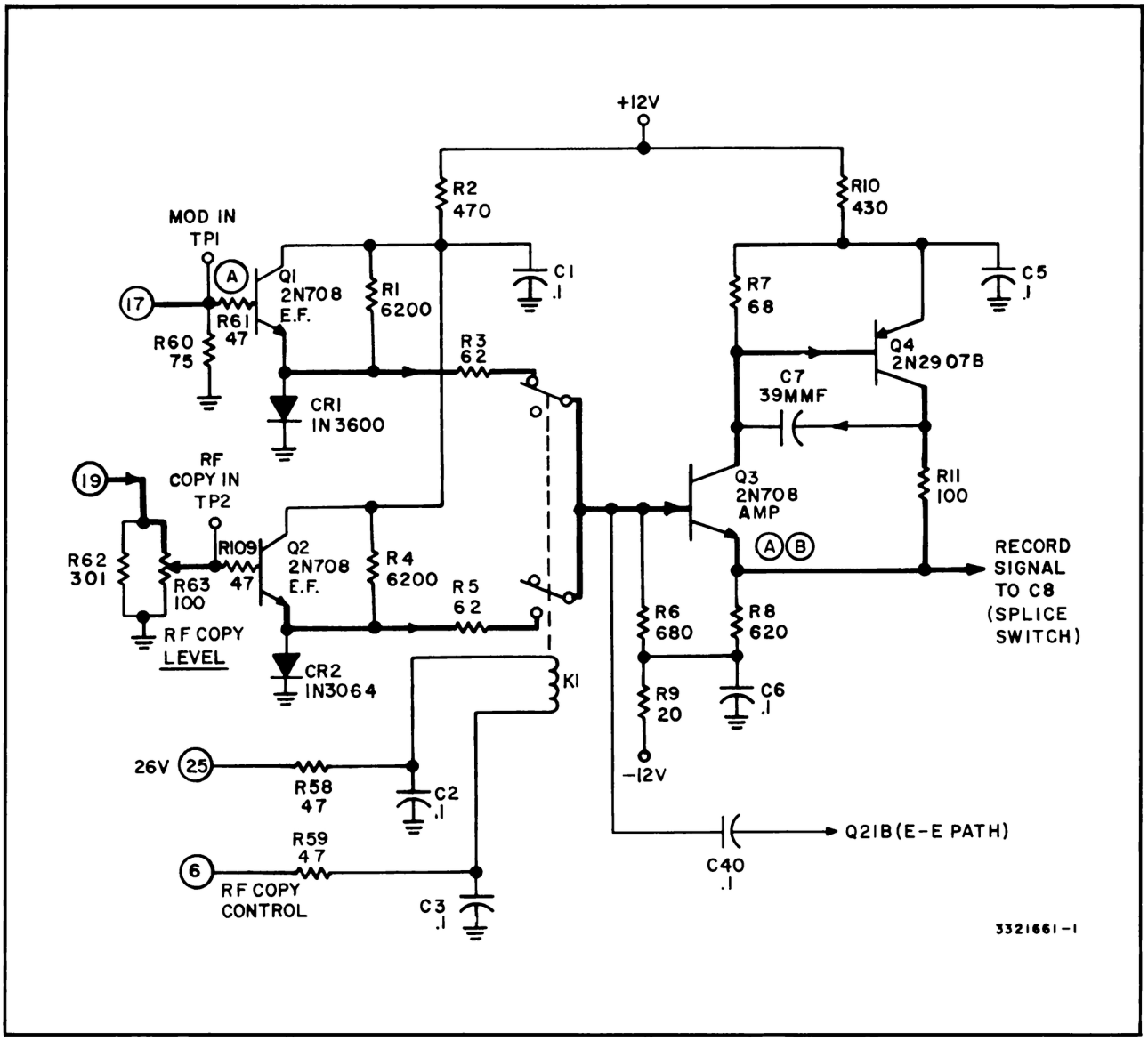
Complete isolation of the rejected signal is accomplished by the diode voltage drop of the silicon diode at the emitter of the transistor in the unselected input. The respective diode of the selected input is cutoff while the counterpart diode is forward biased. This forward bias results in a positive potential that is larger in magnitude than the base-emitter drop of the germanium transistor, thereby back-biasing that transistor.

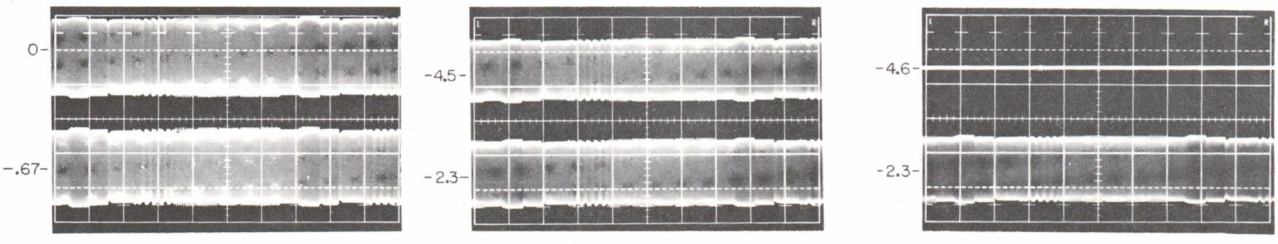
Assume that relay K1 is deenergized. The voltage divider consisting of resistors R2, R1, R3, R6 and R9 places the emitter of Q1 at a negative potential, thereby cutting off diode CR1. At the same time, resistors R2 and R4 place the emitter of Q2 at a positive potential, thereby forward biasing diode CR2 and reverse biasing Q2 which prevents the rf copy from passing. When relay K1 becomes energized, the relay contacts complete the voltage path of the plus 12-volt supply to the minus 12-volt supply through the divider network consisting of R2, R4, R5, R6 and R9, thus cutting off CR2 and forward biasing CR1. This permits the rf copy to pass through relay K1 while inhibiting the record FM signal.

Once through the relay, the selected signal is applied to two points. One is to splice switch control circuits at the base of transisor Q3. The second is to the E-E circuits, through capacitor C40 and to the base of Q21. Each of these circuits is described separately below.

Splice Switch Control

This circuit functions with other splice switching circuits in the machine to stop the recording operation for a precise interval of time so that editing on the tape may be accomplished. See figure 41. Further information on the overall operation of the splice functions may be obtained from instruction book IB-31872.



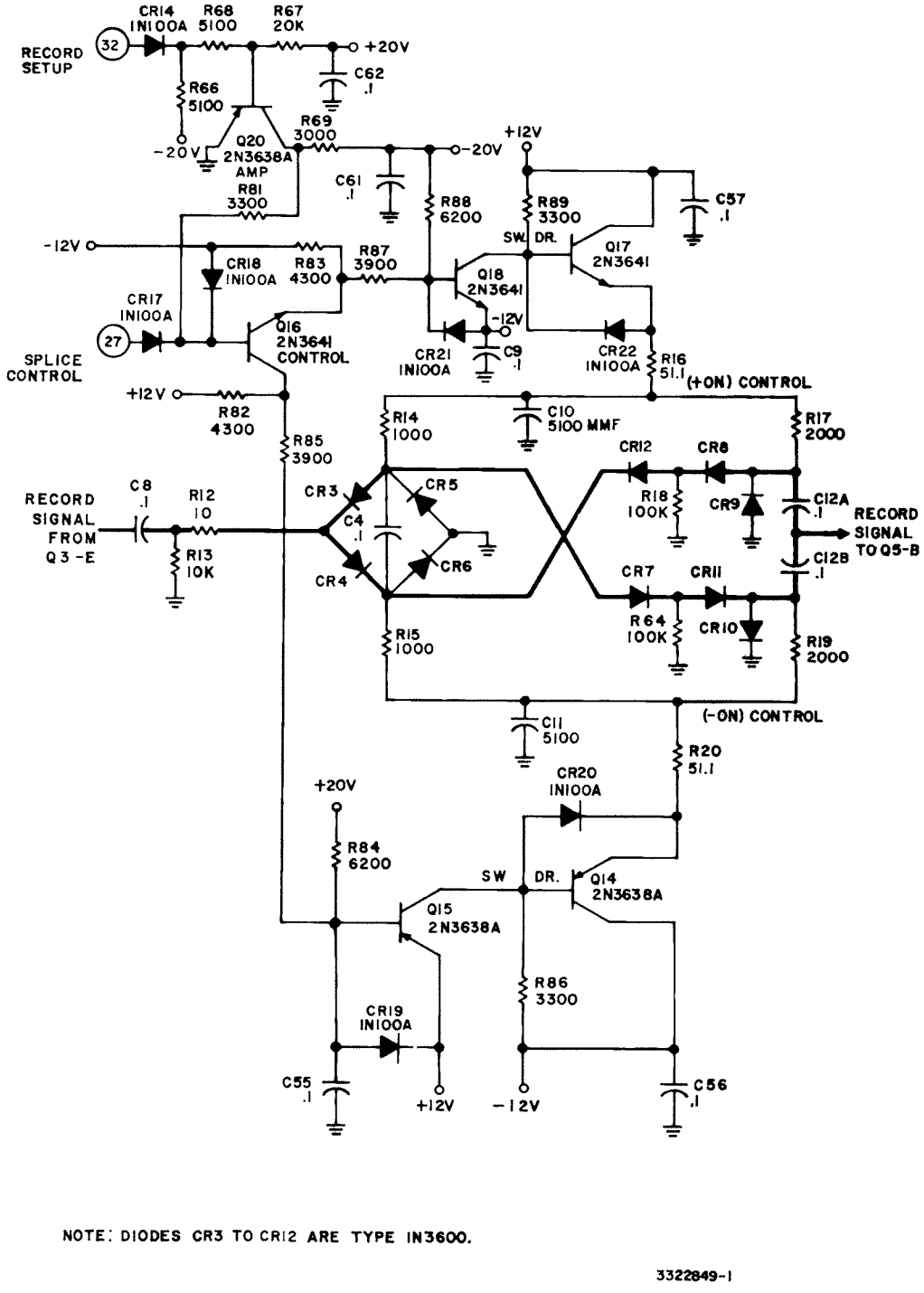


A. Top: TP1
Bottom: Q1 emitter
Both: .1 v/cm, 10 μs/cm
SETUP mode, Highband Standards

B. Top: Q3 emitter
Bottom: Q5 base
Both: .1 v/cm, 10 μs/cm
SETUP mode, Highband Standards

C. Top: Q3 emitter
Bottom: Q5 base
Both: .1 v/cm, 10 μs/cm
STOP mode, Highband Standards

Figure 40—Input Signal Circuits, Schematic Diagram and Typical Waveforms



NOTE: DIODES CR3 TO CR12 ARE TYPE IN3600.

3322849-1

Figure 41—Splice Switch Control Circuits, Schematic Diagram

The splice switch control circuit consists of diode gates that are driven either off or on which causes the FM signal to either be blocked or to commence to the Record Amplifier module. When the gates are closed (off), attenuation in excess of 60 dB is presented to the FM signal at the output of the Record Equalizer module to provide satisfactory isolation for the electronic editing function.

1. Switch Drivers

When the machine is in either RECORD or SETUP modes, a positive level is fed into the module through pin 32 to forward bias diode CR14 and cut off transistor Q20. With Q20 off, diode CR18 is forward biased through resistors R69 and R81, to place the voltage at the base of Q16 more negative than its emitter. Transistor Q16 is thus cut off, which in turn cuts off transistor Q15 due to the increased posiive level on its base. With Q15 cut off, the base of Q14 becomes more negative and transistor Q14 conducts heavily to provide the −"on" control level through its collector-emitter.

Because transistor Q16 is not conducting, the negative level present on its emitter is transferred through resistor R87 to the base of Q18. The negative level holds transistor Q18 cut off and presents a more positive level on the base of Q17. The latter then conducts heavily and supplies the +"on" control level through its collector-emitter. The conduction of Q14 and Q17 turns on the switching diodes and permits FM to pass through the diode gate. (The diode gate is further described below.)

If an electronic splice is to be made, the record/setup positive control level supplied through pin 32 is removed. This allows the base of Q20 to become more negative and causes it to conduct. The sequence of operation through transistors Q14 through Q18 is then reversed and the +"on" and −"on" control levels to the diode gate are reversed. The state of the diodes in the gate is then reversed and the FM signal is blocked.

After the record/setup control level is removed from input pin 32, a positive splice control level is applied to the module through pin 27 by actuating the machine SPLICE switch. This positive level holds transistor Q16 in conduction and inhibits signal flow through the diode gate. When the new information is spliced into the tape electronically, and the machine is returned to RECORD operation, the splice control level remains at pin 27 for the required interval of time. During this interval, the tape is being erased but the record signal is blocked. When one-half second has elapsed (at 15 IPS), the section of tape that was first erased is now in proper position under the headwheel. At this time, the record level on pin 27 becomes negative and the splice signal is recorded on tape.

2. Diode Gate

The diodes in the diode gate are controlled by the control levels supplied from switch drivers Q14/Q15 and Q17/Q18. When FM is to pass through the diode gate (because the machine is in RECORD or SETUP and no splice function is to be performed), the "on" control supplies a minus level through resistor R20 and a plus level through resistor R16. The minus level forward biases diodes CR4, CR12 and CR11, while inhibiting diodes CR5 and CR10. The plus level forward biases diodes CR3, CR7 and CR8, while inhibiting diodes CR5 and CR9.

When FM is to be inhibited from passing through the diode gate, the control levels through resistors R20 and R16 are reversed. This supplies a positive level through R20 to diodes CR6 and CR10, and a negative level through R16 to diodes CR5 and CR9. Diodes CR3, CR4, CR7, CR8, CR11 and CR12 operate as series open switches. Diodes CR5, CR6, CR9 and CR10 function as shunt-shorted switches. This dual action provides a high degree of isolation of the FM signal from its input to output.

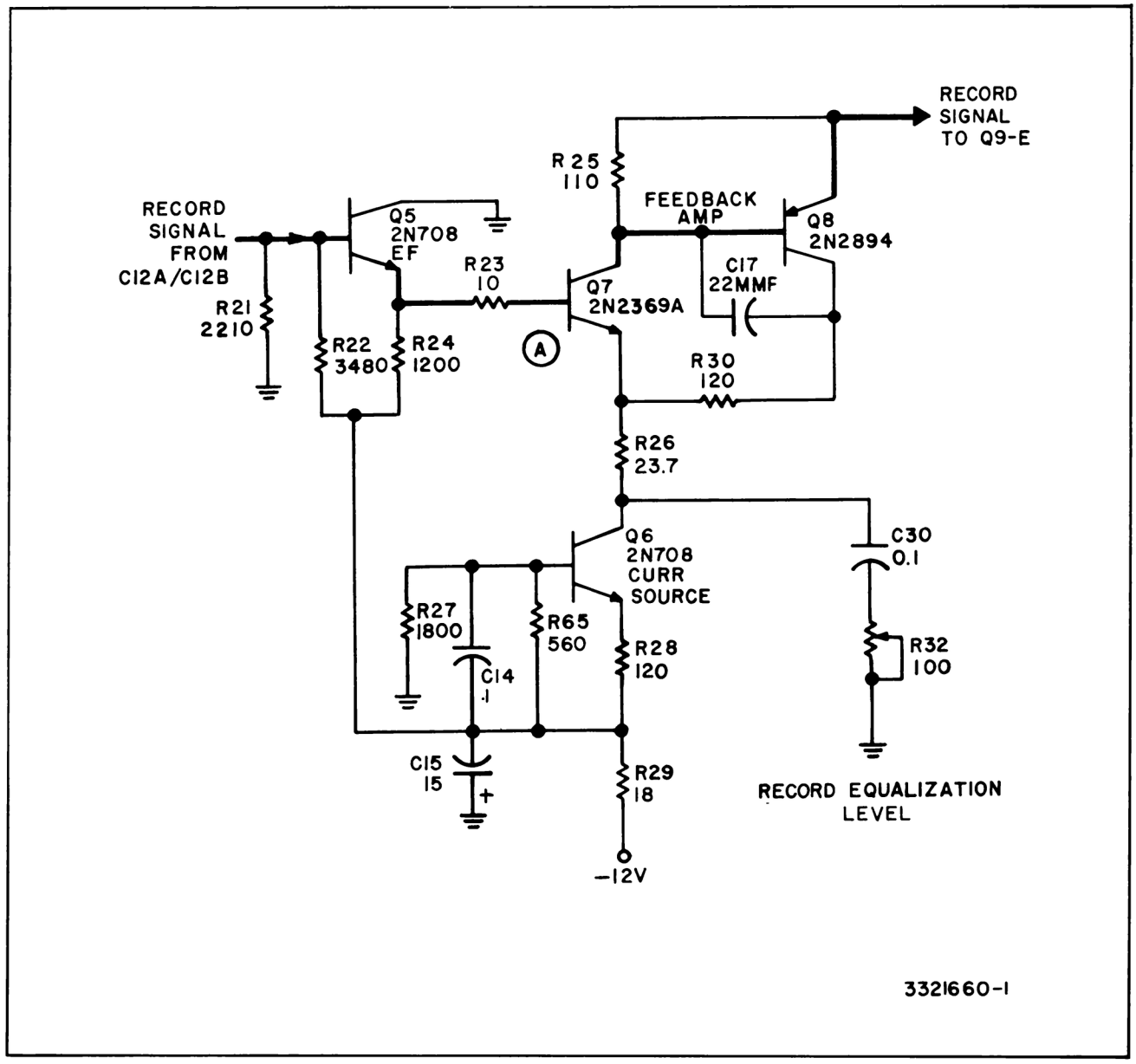
The diode gate operates in push-pull fashion; consequently, any distortion that may be generated by even harmonics is nullified. Capacitors C12A and C12B are matched so that voltage surges caused by the reversing conditions of the diode switch are balanced out.

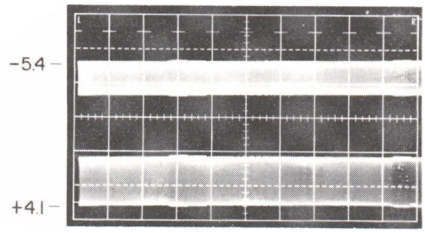
Feedback Amplifier

After passing through the splice switch control circuit, the FM signal is taken from the junction of matched capacitors C12A and C12B and fed to the base of emitter follower Q5, which supplies the signal to the base of Q7 which operates with Q8 to form a feedback amplifier. See figure 42.

Transistor Q6 serves as a high impedance dc current source for feedback amplifier Q7/Q8. The collector of Q6 is connected through isolation resistor R26 to the emitter of Q7. The emitter of Q6 is connected to the minus 12-volt supply through resistors R28 and R29, thus providing a controlled current source for transistor Q7.

The AC gain of the feedback amplifier is controlled by the Record Level potentiometer, R32,





A. Top: Q7 base, 0.2 v/cm
Bottom: Q9 collector, 1 v/cm
Both: 10 μs/cm
SETUP mode, Highband Standards

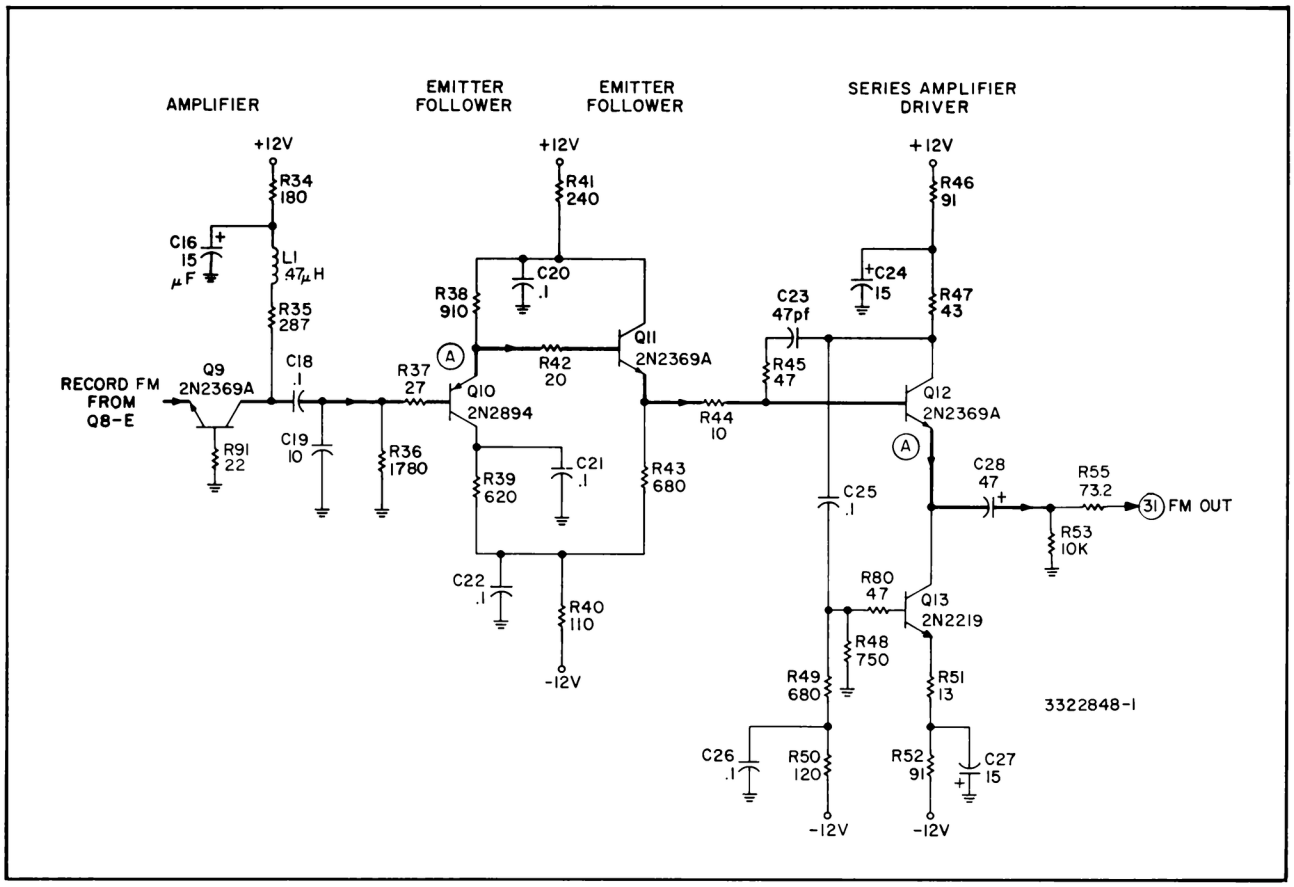
Figure 42—Feedback Amplifier Circuit, Schematic Diagram and Typical Waveforms

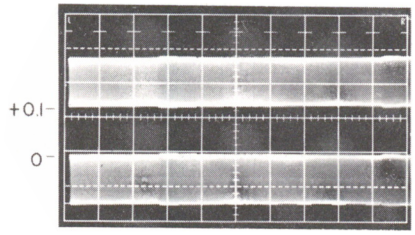
which shunts the high impedance dc current source, Q6. The level is normally set to provide an FM output of the module to the Record amplifier of 0.7 volts peak-to-peak.

Amplifier and Driver

FM from the emitter output of Q8 is supplied to the emitter of Q9, which operates as a common-base amplifier with a low impedance. The input to Q9 is a signal current that increases linearly with frequency. The output is taken from the collector of Q9 and appears across inductor L1 with resistor R35. This input signal and circuitry on the collector of Q9 causes the output voltage to increase linearly with frequency. See figure 43.

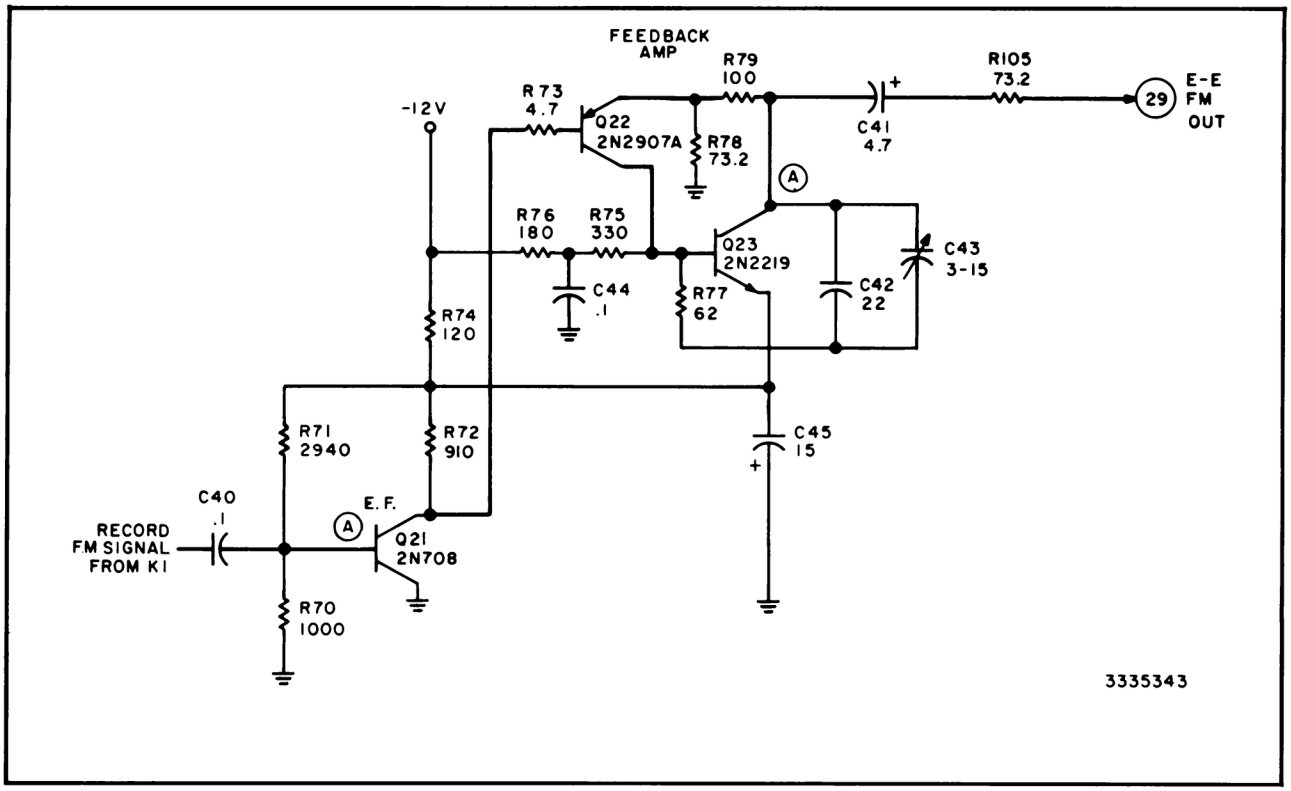
The signal is ac-coupled through capacitor C18 to the base of Q10. The emitter output of Q10 is supplied to the base of transistor Q11 to result in a cascaded emitter follower configuration with Q10 and Q11. The emitter output from Q11 is coupled through islation resistor R44 to series amplifier Q12/Q13.

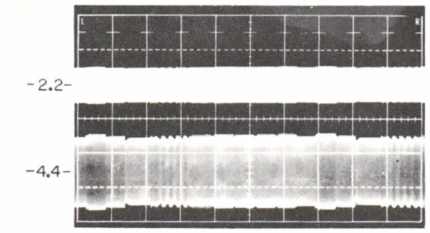




A. Top: Q10 emitter
Bottom: Q12 emitter
Both: 1 v/cm, 10 μs/cm
SETUP mode, Highband standards

Figure 43—Amplifier and Driver, Schematic Diagram and Typical Waveforms





A. Top: Q21 base
Bottom: Q23 collector
Both: .2 v/cm, 10 μs/cm
SETUP mode, Highband Standards

Figure 44—E-E Path Circuitry, Schematic Diagram and Typical Waveforms

Transistors Q12 and Q13 function as line drivers for the FM output from the module. The input signal to the base of Q12 is amplified through the latter and fed out from its emitter. The collector output of Q12 is fed to the base of Q13 through coupling capacitor C25 and resistor R80. The collector output of Q13 is joined with the emitter output of Q12 to provide a high current output through capacitor C28. The output point of C28 is fed to the terminating resistor R55. This in turn, is connected to the output from the module to the Record Amplifier module. The impedance at pin 31 is 75 ohms, with an output level of one volt peak-to-peak (nominal) when terminated, and with a carrier frequency of 8.5 MHz.

E-E FM Path

The E-E FM circuits amplify the input FM or rf copy signal after passing through their appropriate emitter follower and relay K1. The amplified signals then becomes the electronic-to-electronic (E-E) signal that is used to check the FM system without passing through the headwheel and its associated input/output circuits.

Input to the EE circuit is provided from the parallel connection point supplied at the center arm of relay K1 contacts. This same point supplies the input to emitter follower Q3 which feeds FM to the splice switch (described above). The E-E FM circuit input is ac-coupled through capacitor C40 to the base of emitter follower Q21. See figure 44.

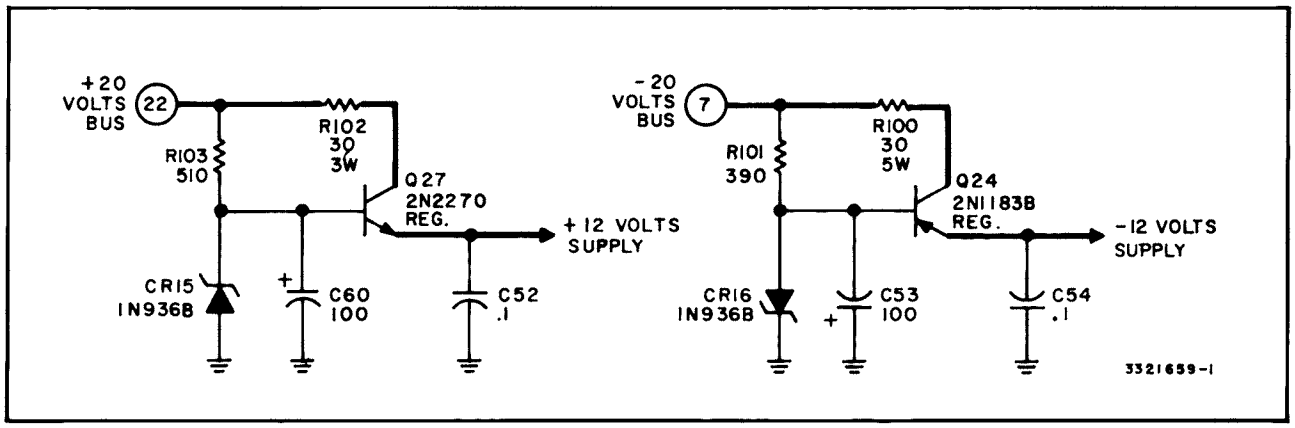


Figure 45—Voltage Regulators, Schematic Diagram

The output of Q21 is supplied to the base of Q22, which with transistor Q23, forms a feedback amplifier. This feedback amplifier has a gain that compensates for attenuation of the input signal through transistor Q1 (or Q2), voltage divider resistors R3 and R6 (or R5 and R6), emitter follower Q21, and the voltage divider consisting of the output resistors and terminations in the modules from pin 29. The output from pin 29 is supplied to the FM Reference module. Trimmer capacitor C43 is factory-adjusted to obtain a flat response of plus or minus 0.2 dB in the range of 1.0 MHz to 14 MHz.

Voltage Regulators

Two series voltage regulators are used in the module, one for the plus 12-volt supply and the other for the minus 12-volt supply. See figure 45. Plus 20 volts is supplied from the machine bus through pin 22 of plug P1 and applied to the collector of series regulator transistor Q27 through voltage dropping resistor R102. The base of Q27 is held at a stable voltage by Zener diode CR15. The base-emitter drop of Q27 provides the required plus 12 volts at the emitter of Q27. Capacitor C60 effectively provides a large amount of filtering due to the gain of transistor Q27. Capacitor C52 filters out rf interference from the line (originating in the module) to prevent it from being fed into the regulator.

The minus 12-volt supply regulator operates similarly to the plus 12-volt supply regulator. However, in this regulator, the Zener diode has its cathode connected to ground because the voltage breakdown is in a negative direction. The output from transistor Q24 is taken from its emitter and fed to the module as the minus 12-volt supply.

ADJUSTMENTS

Chassis adjustments on the Record Equalizer module have been carefully set at the factory and should not be disturbed unless positive determination has been made that all other possible defects are corrected. Settings for trimmer capacitors C43 and C47, and potentiometer R32 have been sealed with red or blue sealing compound to indicate that these are critical factory adjustments that should not be disturbed. If service is required, contact your RCA field representative.

RF Copy Level

The RF COPY LEVEL potentiometer (R63) on the module front panel is adjusted while the machine is operating in RF COPY mode. If required, this setting may be made by monitoring the level on test point TP2 and setting the control to obtain a level of 250 millivolts peak-to-peak.

RECORD AMPLIFIER MODULE

CIRCUIT DESCRIPTION

General

The record amplifier module consists of a very high gain amplifier which is common to all four record channels, and four identical sets of amplifiers, one for each channel which are housed in a single module. For the purposes of description only one of these record amplifier channels will be discussed. Refer to the block diagram, figure 46.

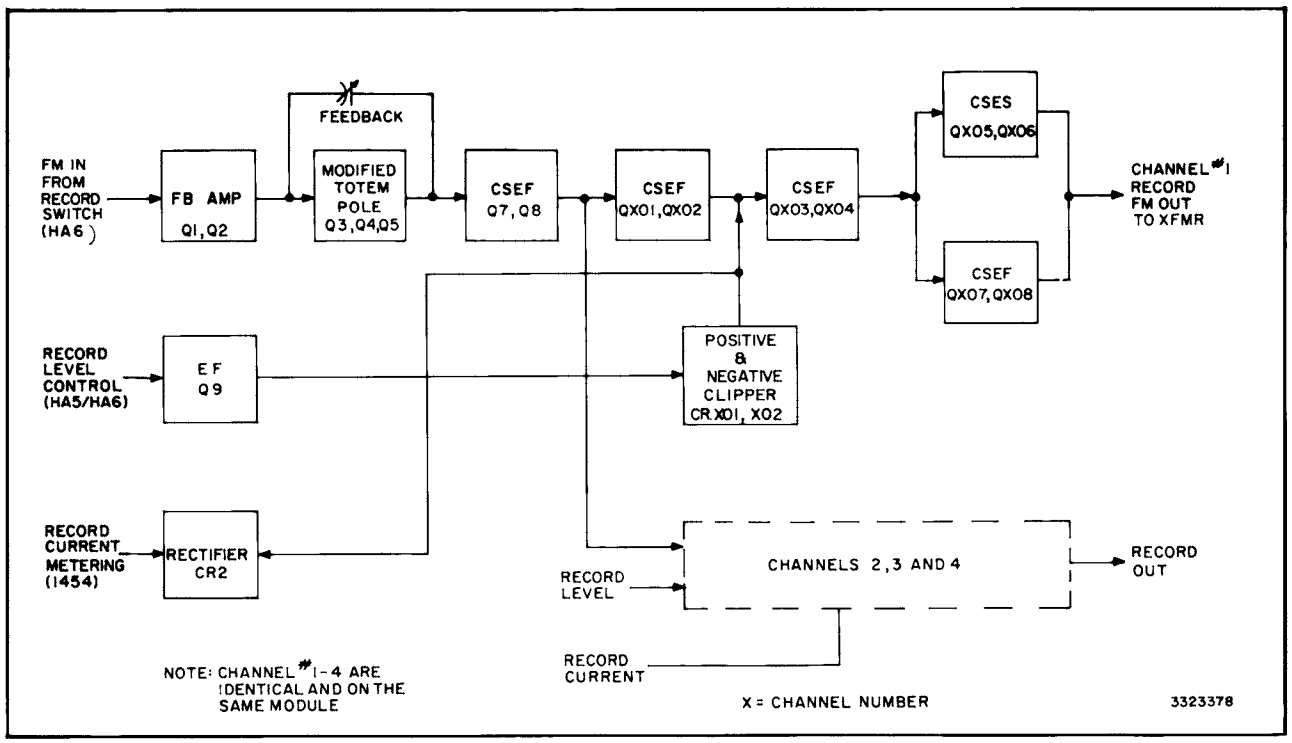


Figure 46—Record Amplifier Module, Block Diagram

Amplifier Section

The FM signal from the record switch module is fed into the module at P1-17 to the base circuit of transistor Q1 (part of a feedback amplifier). See figure 47. Q1 and Q2 form to constitute a unity gain feedback amplifier. The ratio of resistors R6 and R3 are essentially the gain controlling components of the circuit. The low output impedance of the unity gain amplifier permits direct coupling to the modified feedback amplifier Q3, Q4 and Q5. In addition to the low impedance feature, Q1 and Q2 provide isolation from the output circuitry of the record switch module.

Transistors Q3, Q4 and Q5 form a high gain feedback amplifier. The frequency response of this amplifier is factory adjusted by high frequency compensating capacitor C5, to be flat over the frequency band of interest.

The output of transistor Q5 is capacitively coupled through C12 to the base circuit of complementary symmetry emitter follower transistors Q7-Q8. Resistors R23 and R26 form a voltage divider which provides +25 volts bias for the FM signal. Isolation and distribution is accomplished at this stage. The FM signal is distributed to the four identical record channels.

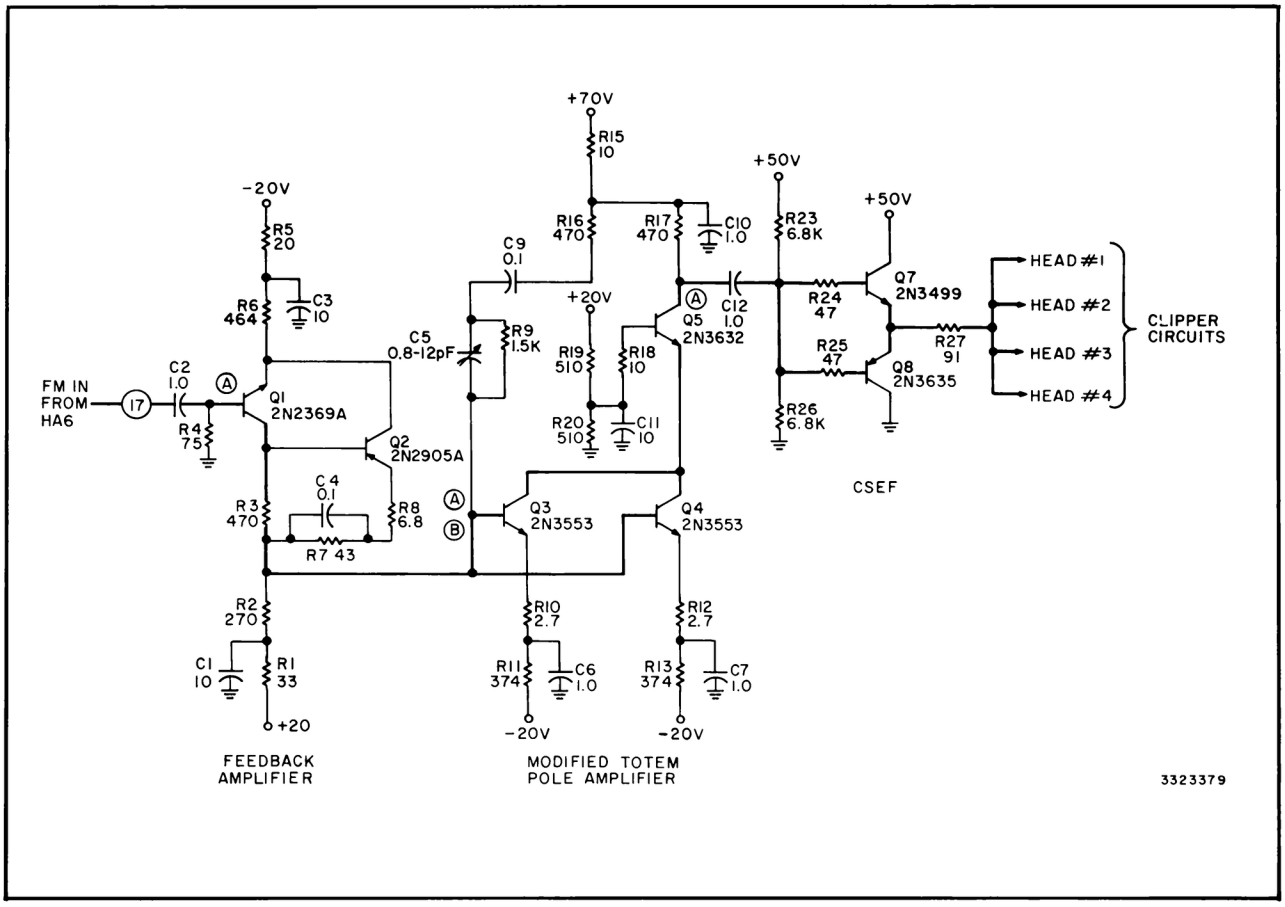
Level Control and Output

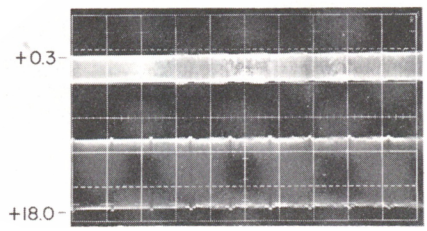
As shown on figure 48, complementary symmetry emitter follower QX01-QX02 provides interchannel isolation. The signal at the base of the CSEF is approximately 40 volts peak-to-peak and is centered about +25 volts. The FM signal at the base of QX03-QX04 is dependent upon the condition imposed by the position of the RECORD CURRENT potentiometer and the positive and negative clipper, CRX01 and CRX02. CRX02 prohibits the signal on the base of CSEF QX03-QX04 from going below ground potential. The potential at the base of Q9, via P1-14 from the RECORD CURRENT potentiometer on the FM reference or record switch module, determines the positive clipping level. The resulting output from QX03-QX04 is determined by the setting of the RECORD CURRENT control.

The FM signal is fed through CSEF QX03-QX04 which provides sufficient current to drive the two CSEF circuits, QX05-QX06 and QX07-QX08. These two CSEF circuits are required to drive the record head transformer on the FM preamplifier module.

Record Head Current Metering

Record head current sampling is accomplished by the rectification of the FM signal at the base of CSEF QX03-QX04 by the circuit consisting of diode CR2, resistor R28, and capacitor C14. Diode CR2 permits the positive half of the FM signal to charge C14 which produces an average dc voltage in relation to the amplitude of the signal.





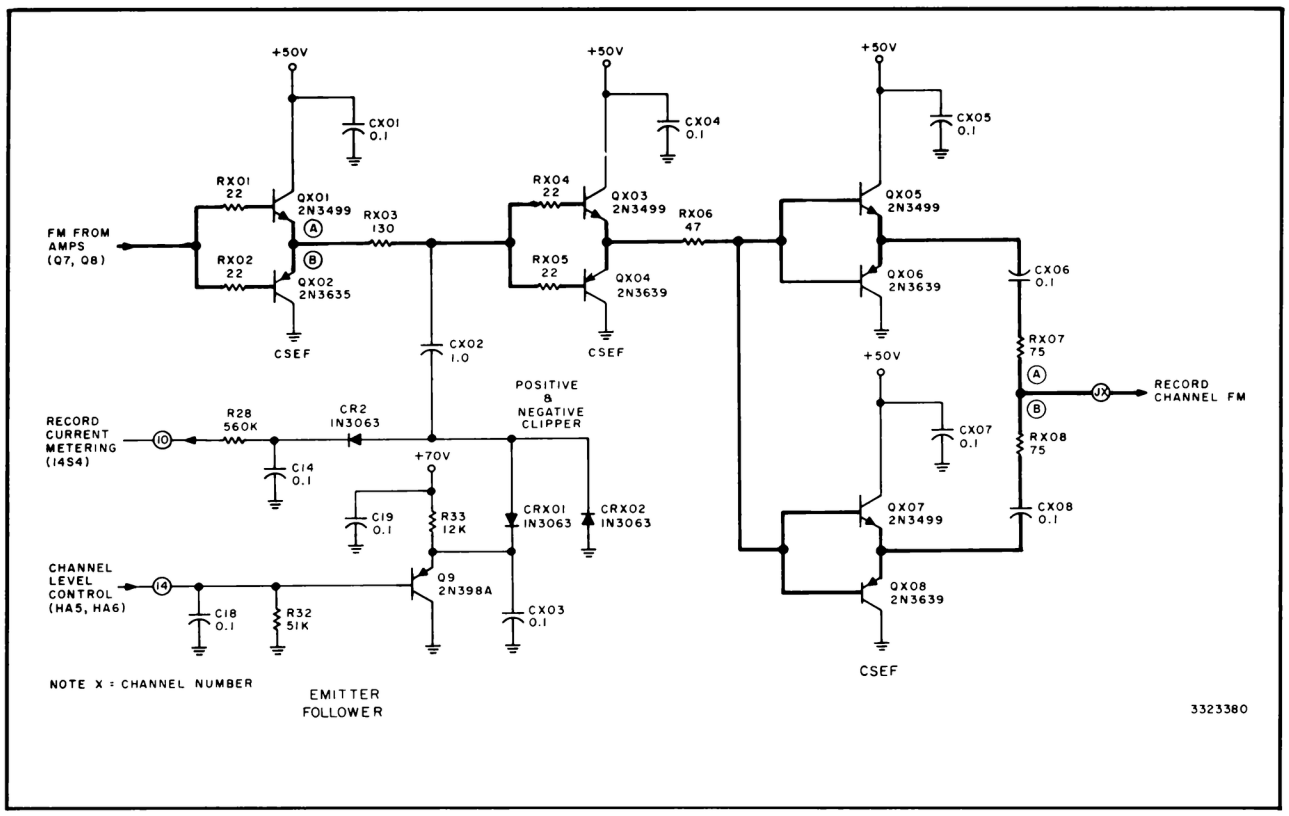
A. Top: P1 pin 17, 1 v/cm
Bottom: Q5 collector, 20 v/cm
Both: 0.05 ms/cm
SETUP mode

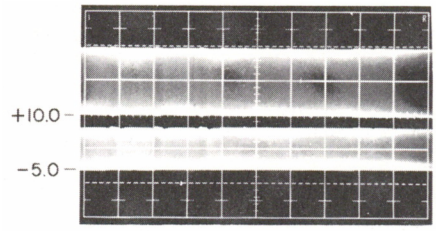
Figure 47—Feedback Amplifiers, Schematic Diagram and Typical Waveforms

The voltage resulting from the rectifier is fed via P1-10 to the RECORD CURRENT meter and indicates the relative current supplied to the head during recording. A switch in the meter circuit provides a means of observing the relative record current for each record head channel.

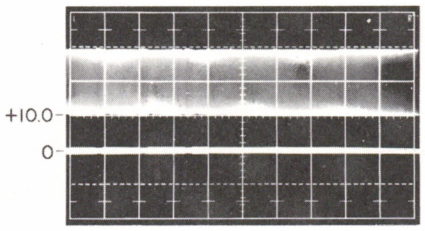
ADJUSTMENTS

Frequency response adjustments on each Record Amplifier module have been carefully set with special test equipment at the factory. Trimmer capacitor C13 and variable conductor L7 have been locked at their adjustment settings with a red or blue sealing compound signifying a critical adjustment that should not be attempted in the field. If service is required, contact your RCA field representative.





A. Top: QX02 emitter, 20 v/cm
Bottom: RX07/RX08, 10 v/cm
Both: 50 ms/cm
Max. drive to record heads



B. Top: QX02 emitter, 20 v/cm
Bottom: RX07/RX08, 10 v/cm
Both: 50 ms/cm
Min. drive to record heads

Figure 48—Heads #1 thru #4 Clipper Circuit, Schematic Diagram and Typical Waveforms

FM PREAMPLIFIER MODULE

CIRCUIT DESCRIPTION

General

In the playback mode of operation, the FM Preamplifier module provides amplification of the FM signal supplied by the heads. The module furnishes the proper impedance match between the heads and the Playback Amplifier modules.

The FM Preamplifier module is physically located as close to the actual playback heads as practical. This ensures that signal loss as a result of transmission line impedance and noise are kept to a minimum in the early stages.

Each preamplifier circuit employs a separate group of symbol numbers for the items used in that circuit as illustrated in figure 49. Channel 1 preamplifier symbols start with 100, channel 2 with 200, channel 3 with 300, and channel 4 with 400. Since there are four identical playback preamplifiers on this module, only one channel will be described in this section.

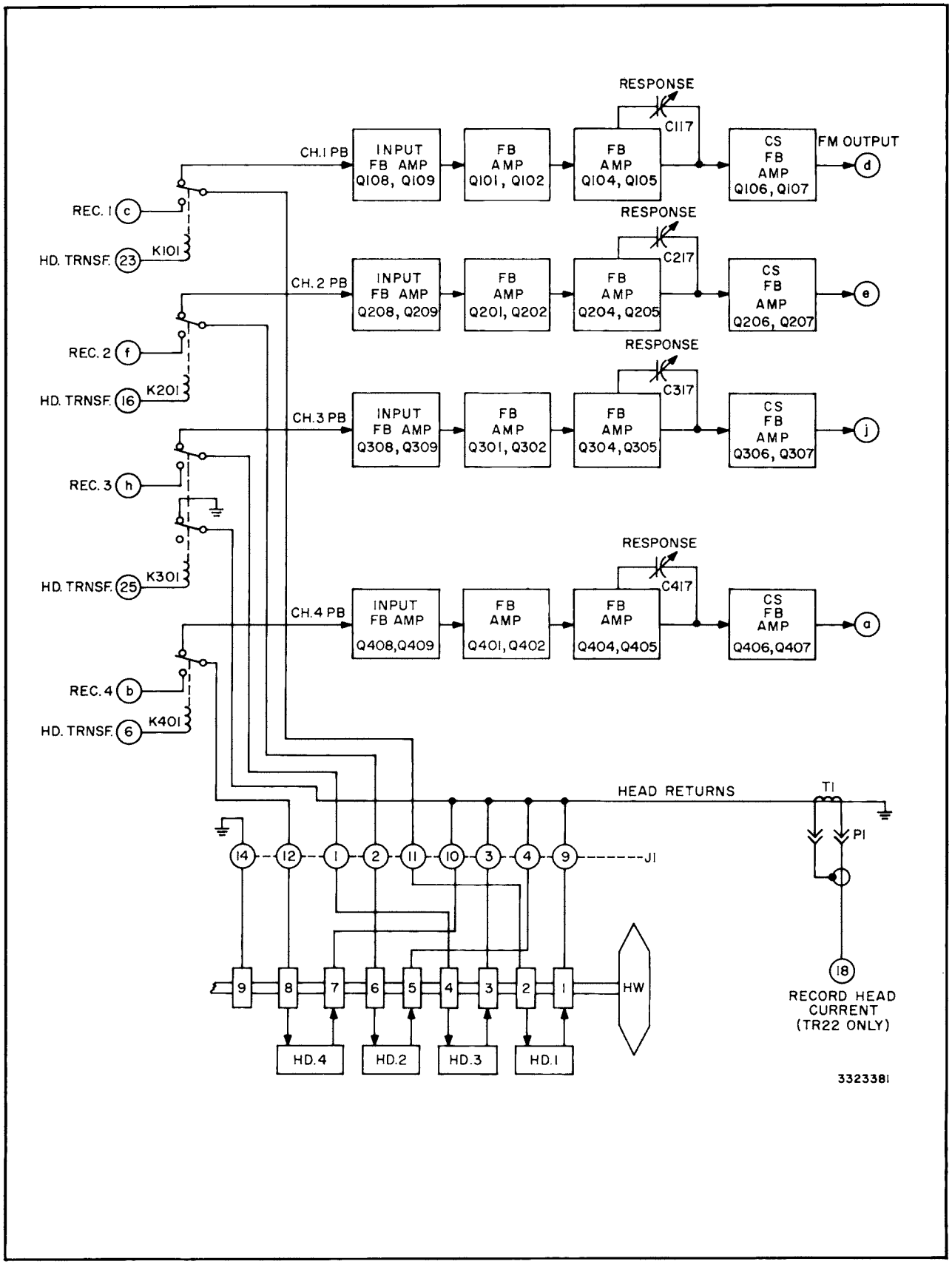


Figure 49—FM Preamplifier Module, Block Diagram

Each preamplifier channel consists of an input circuit that maintains a constant low impedance, a feed back amplifier, another feedback amplifier with circuitry that effectively boosts the high frequencies, and a complementary symmetry feedback amplifier that provides unity gain as well as a low impedance output to the playback amplifier.

When the machine is operating in the RECORD mode, FM signals from the four Record Amplifier modules are routed to the FM Preamplifier module through the record transformers by the head transfer relays K101, K201, K301, and K401 to the heads. Each relay is located near the front of the module and has provisions for transferring the signal between Record and Playback for its associated channel. The relays are energized simultaneously during the RECORD mode by a common connection point that is routed through the Preamplifier Filter module.

As shown in the block diagram of the FM Preamplifier, figure 49, each brush and slip ring has a separate wire to transfer the head signal into the module, and another wire to return the ground for each head. These are all fed into the module through jack J1, where the head ground-return wires are joined together and connected to ground through current transformer T1. The transformer develops a voltage which is proportional to the record current. This voltage is then routed to the Indicator module for current metering in the TR-22HB. In the TR-4HB and TR-50 this transformer is shorted out all the time.

During playback operation, transformer T1 is shorted out by the second set of contacts in relay K301, thus minimizing crosstalk effects that are caused by the common reflected impedance of the current transformer. Individual record head current are monitored in the TR-4HB/50 tape machines through a rectifier stage to a meter. Subsequent circuit descriptions are all part of the playback operation function of the module.

Input Feedback Amplifier

As illustrated on figure 50, the input feedback amplifier is composed of Q8 and Q9. (Since all four FM preamplifier channels are identical, the prefix number has been dropped for the description.) In the playback mode of operation, the REC/PB relays are in the de-energized state which permits the FM signal on tape to be fed to the base of transistor Q8.

Q8, Q9 form to make a feedback pair amplifier. The properties of a feedback pair amplifier can be obtained by sensing the output voltage of Q7 and feeding back this voltage in parallel with the input

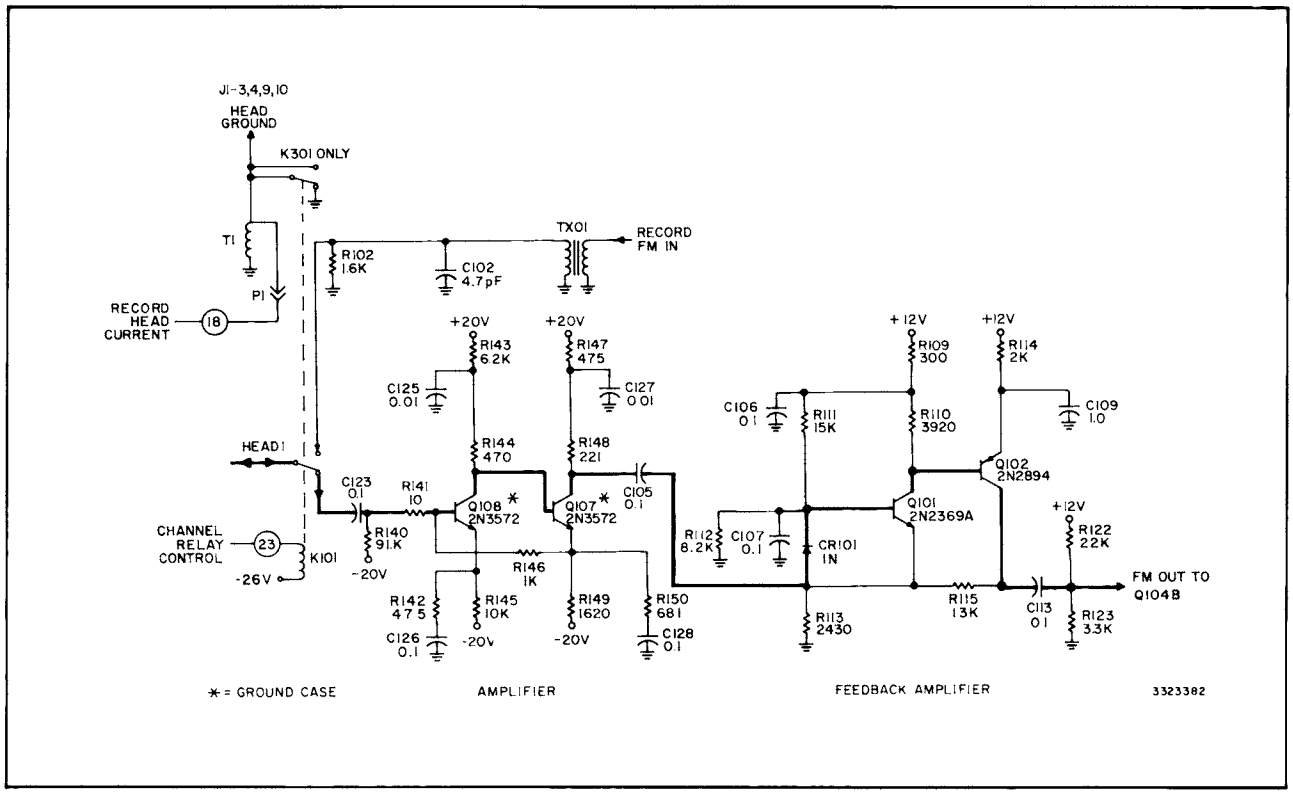


Figure 50—Switching and Feedback Amplifiers

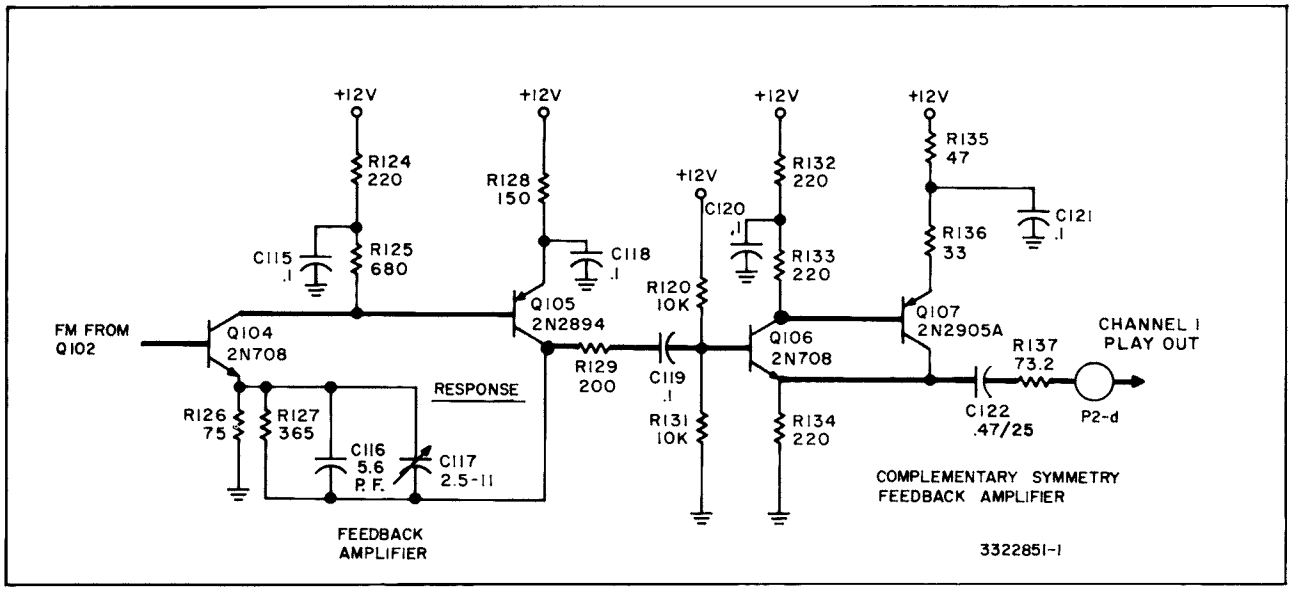


Figure 51—Feedback Amplifiers

signal. The shunting effect of the feedback resistor R46 causes the apparent closed-loop impedance to be reduced. In other words, this type of amplifier has low input and low output impedance and supplies an output voltage in proportion to the input current. Using the negative feedback from the emitter of Q9 through feedback resistor R46 to the base of Q9, the input impedance is reduced.

For the circuit used in the high band machines, the value of input impedance is approximately 150 ohms. Comparing this impedance with that of the head which is approximately 5 to 6K ohms, it is important to note that an increase in current at the head is greatly increased at the input to the amplifier. This current drives the second half of this type amplifier to produce a signal at the output of transistor Q9. With a relatively small magnitude of input current, a proportionally greater magnitude of output signal is attainable.

Another advantage to this type amplifier is that since the ratio of head impedance to input impedance is greater than 10:1, any appreciable change in head impedance will not, for all practical purposes, affect the input signal magnitude.

Feedback Amplifiers

The FM signal is taken from the collector of Q9 and coupled through capacitor C5 to the emitter of Q1, which presents a very low impedance to the Q9 output. Transistors Q1 and Q2 form a feedback amplifier. Feedback is supplied from the collector of Q2 through resistor R15 to the emitter of Q1. See figure 50.

The collector output from Q2 is ac-coupled through capacitor C13 to the base of Q4. The latter functions with Q5 to form a feedback amplifier having a gain of approximately six. Feedback is provided from the collector of Q5 through capacitors C16 and C17 with resistor R27. Trimmer capacitor C17 is adjusted at the factory to provide a flat frequency response of ±0.05 dB from 1.0 MHz to 14 MHz. See figure 51.

The signal output of Q4 and Q5 is taken from the collector of Q5 and is ac-coupled through resistor R29 and capacitor C19 to the base of Q6. The latter operates with Q7 to form a complementary emitter follower. The gain of these two transistors is slightly less than unity, with an output impedance of approximately one ohm. Their output is supplied from the collector of Q7 and coupled to connector P2 through capacitor C22 and resistor R37. This RC circuit fixes the channel output impedance at 75 ohms.

Operating power to the FM Preamplifier module is filtered in the Preamplifier Filter. The plus 12-volt supply is switched off during RECORD mode of operation. Output from current transistor T1 is connected to plug P2-A and from there is routed to the indicator head current metering circuit on the Indicator module (TR-22HB only).

MAINTENANCE

Typical Voltage Levels

Waveforms are not supplied with the schematic diagrams of the FM Preamplifier module because the signal indications are fm sine waves. Instead, dc

TABLE 6—FM PREAMPLIFIER VOLTAGES

Item	*Plus DC Volts*		
	Emitter (Cathode)	*Base (Grid)*	*Collector (Plate)*
Q101	3.2	3.8	9.4
Q102	10.0	9.4	4.2
Q104	0.74	1.32	9.8
Q105	10.2	9.8	4.0
Q106	5.0	5.6	9.4
Q107	10.0	9.4	5.0

voltage levels for the amplifier stages are listed in the following table to assist in troubleshooting.

ADJUSTMENTS

The FM Preamplifier module has been carefully adjusted at the factory for a flat frequency response of ±0.05 dB from 1.0 MHz to 14 MHz. The associated trimmer capacitor adjustment has been locked in place with red or blue sealing compound to indicate that it is a critical factory adjustment and should not be disturbed. If service is required, contact your RCA field representative.

PLAYBACK AMPLIFIER MODULE

CIRCUIT DESCRIPTION

General

To accommodate the four channels of a quadruplex system, two separate modules are used. One module is used for the odd numbered channels and another module is used for the even numbered channels. See figure 52. Each channel receives an input from one of the four playback channels on the FM preamplifier module. The playback module contains playback compensation which is provided by cosine equalization of frequency response of the FM signal. Cosine equalization permits handling of the FM signal frequencies with a constant group delay that does not distort or alter the original phase relationship of the frequency component of the reproduced FM signal. In addition, the signals from the two channels on the playback module are combined internally by a 4X2 FM switcher which is timed by a signal from the FM Switch module.

Since all four playback channels on the two modules are identical, only one will be described. Also, since the two FM switch circuits on the modules are identical, only one will be discussed.

Input Amplifier and Delay Line Driver

Input to the amplifier Q1 is fed into the module from the FM preamplifier via pin 17 (pin 19 for the other channel) and coupled through capacitor C1 to the base of Q1. Potentiometer R2 varies the amplitude of the incoming signal. Amplifier Q1 in conjunction with transistor Q2 form a circuit that functions in a similar manner as a complementary symmetry emitter

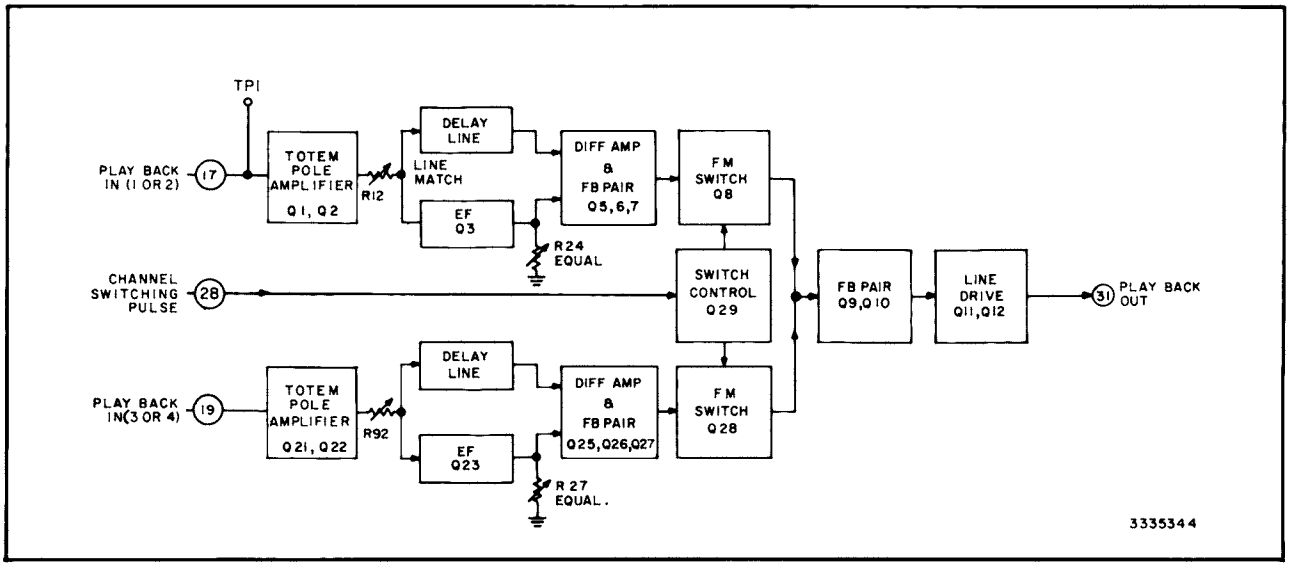


Figure 52—Playback Amplifier Module, Block Diagram

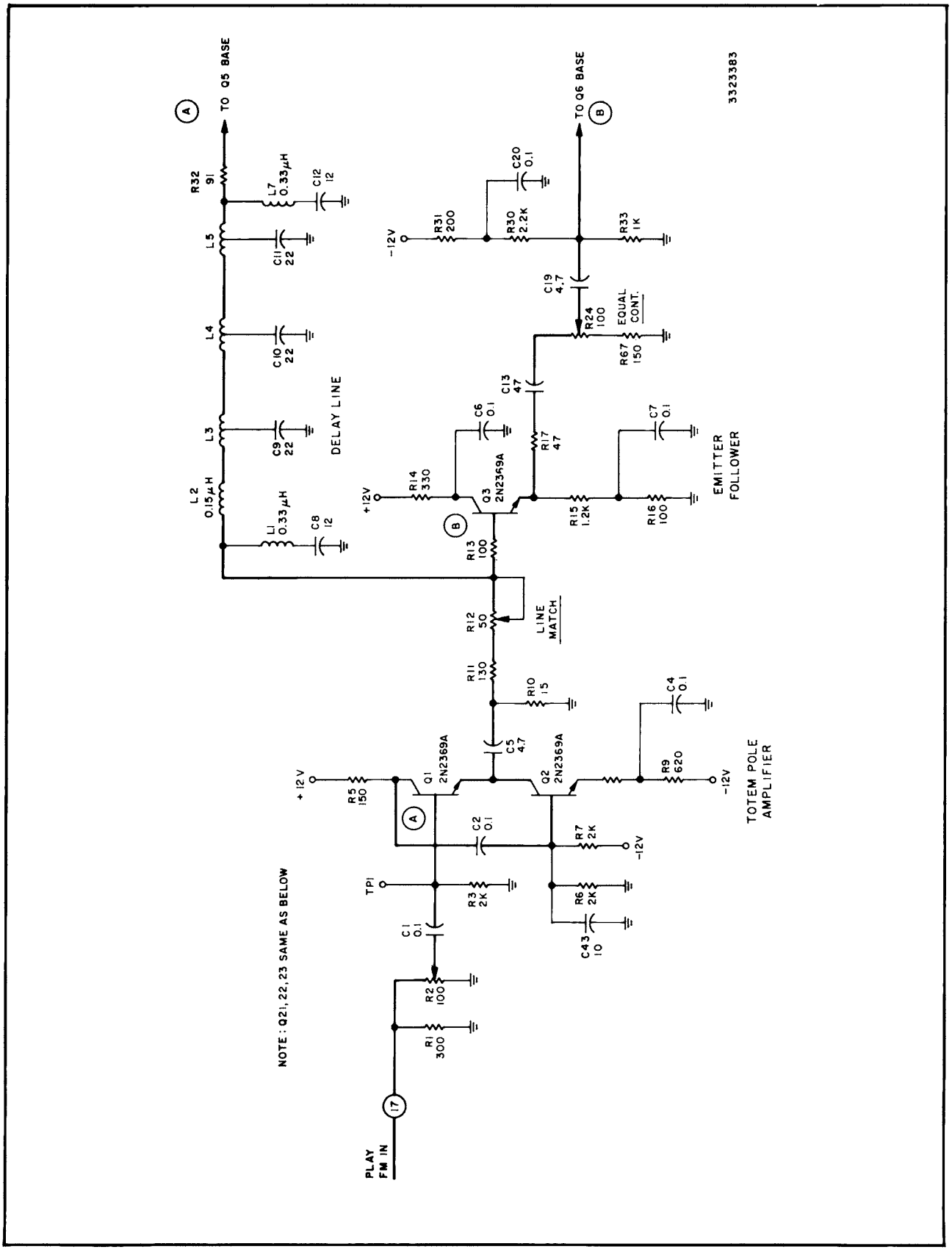
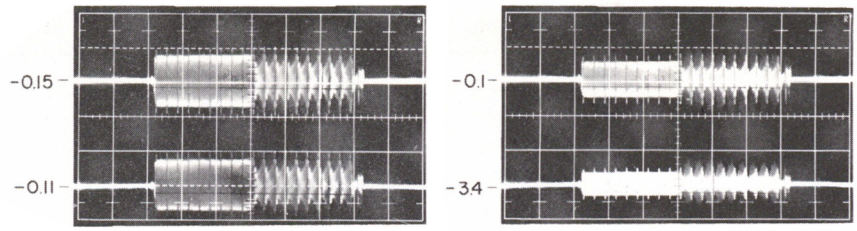


Figure 53—Amplifier Section with Delay Line, Schematic Diagram and Typical Waveforms

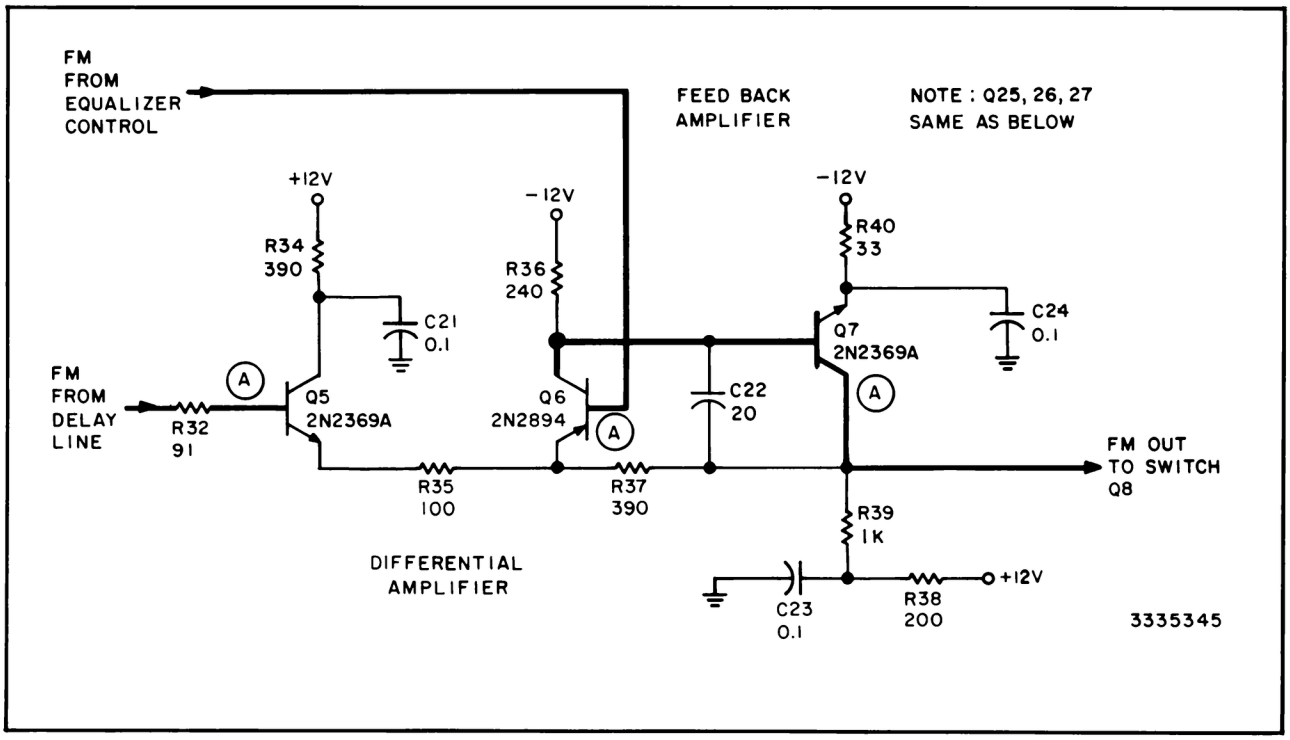


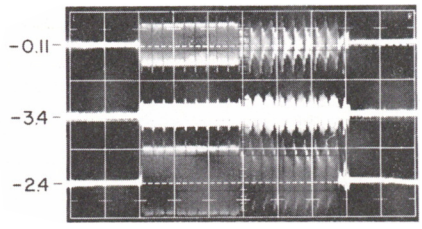
A. Top: Q1 base
Bottom: Q5 base
Both: 0.1 v/cm, 0.2 ms/cm

B. Top: Q3 base
Bottom: Q6 base
Both: 0.1 v/cm, 0.2 ms/cm

All waveforms in PLAYBACK mode.

Figure 53—Amplifier Section with Delay Line, Schematic Diagram and Typical Waveforms (Continued)





A. Top: Q5 base
Middle: Q6 base
Bottom: Q7 collector
All: 0.1 v/cm, 0.2 ms/cm
Machine in PLAYBACK mode

Figure 54—Difference Amplifier and Feedback Amplifier, Schematic Diagram and Typical Waveforms

follower circuit, thus unity gain is achieved through the stage. As seen on figure 53, transistors Q1-Q2 provide sufficient current to drive the delay line and the emitter follower transistor Q3.

The output junction of Q1-Q2 also provides a low impedance to the delay line sending-end. Potentiometer R12 LINE MATCH, is adjusted to the characteristic impedance of the delay line thereby obtaining a flat response at the receiving end.

Delay Line and Equalization

The delay line and its associated equalization circuits produce conditions that permit processing of the FM playback signal without distorting or altering the phase characteristics of the signal and providing shaping of the amplitude response to a prescribed criterion.

Referring to figure 53, the output of amplifier Q1-Q2 is coupled through capacitor C5, resistor R11 and potentiometer R12, and is split into two paths, one is fed to the base of transistor Q3 and the other is fed to the junction of inductors L1 and L2 of the delay line. Transistor Q3 is an emitter follower which provides isolation between the delay line and the equalization control.

The delay line essentially has a constant delay of 16 nanoseconds and a cut-off frequency of 32 megahertz. It is an amplitude responsive device which varies the amplitude of the incoming FM signal. Transistors Q5 and Q6 constitute a differential amplifier which has for its inputs the undelayed signal on Q6 and the delayed signal on Q5. See figure 54. The differential amplifier by virtue of its operation produces an output which is attenuated at the low fre-

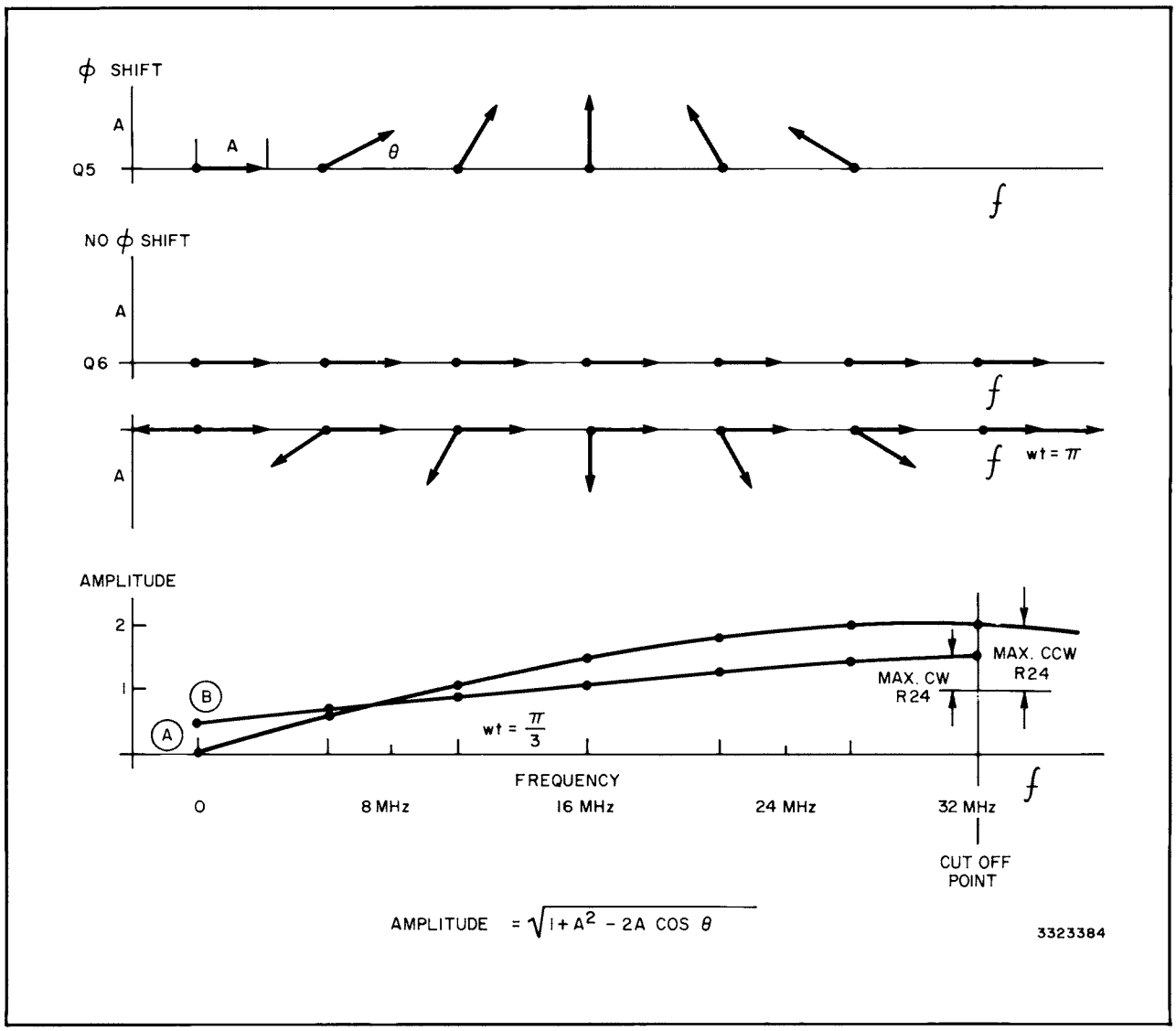


Figure 55—Cosine Equalization

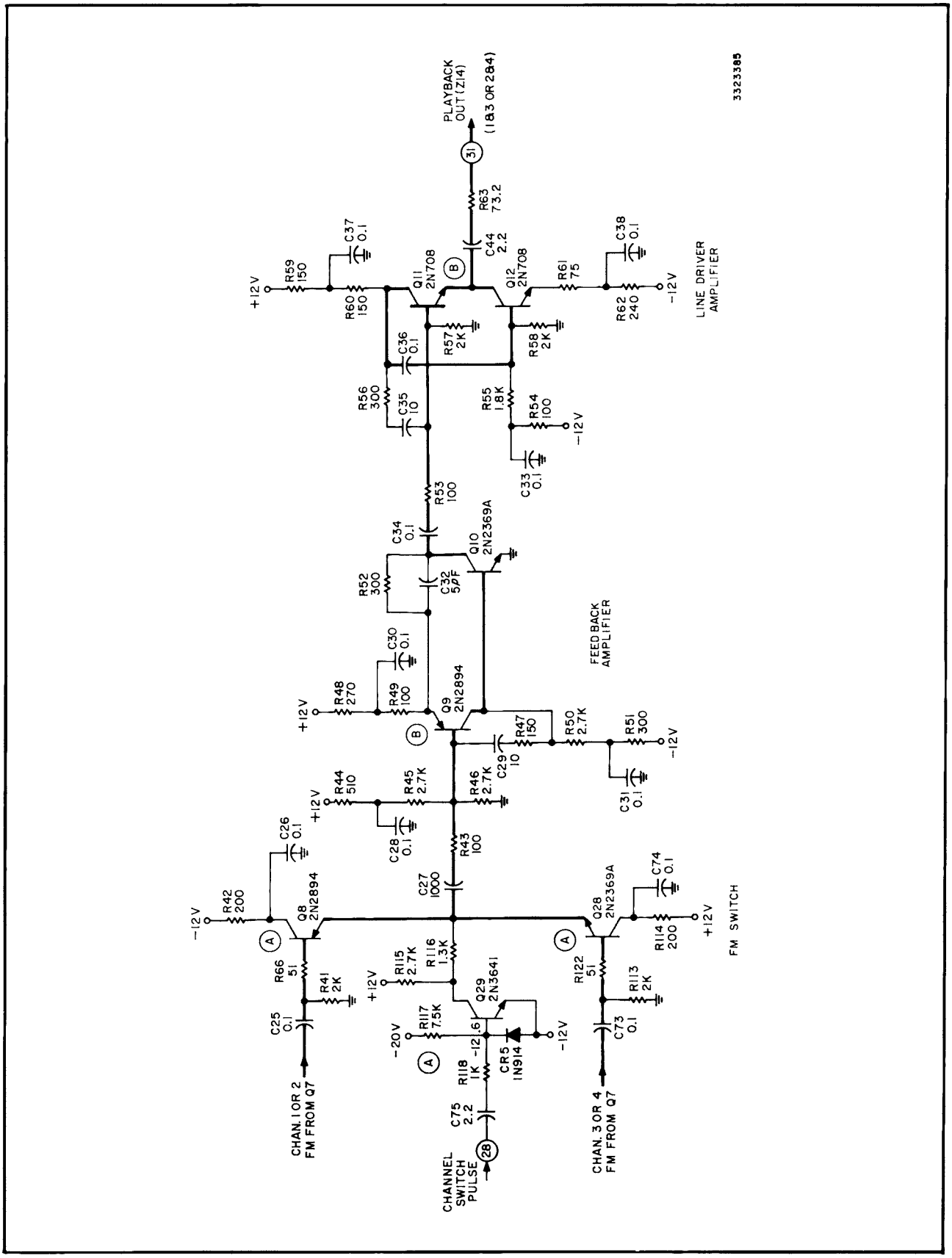
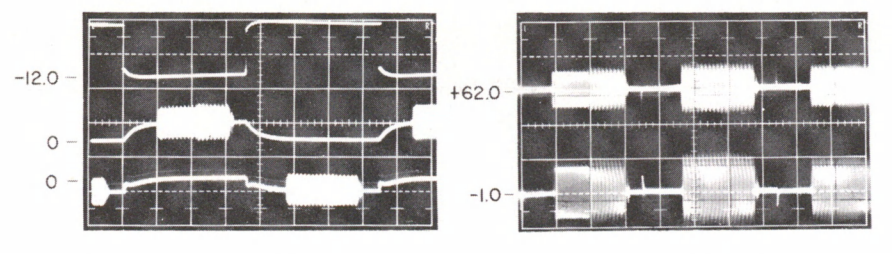


Figure 56—Channel Switching and Output, Schematic Diagram and Typical Waveforms



A. Top: Q29 base, 1 v/cm
Middle: Q8 base, 0.2 v/cm
Bottom: Q28 base, 0.2 v/cm
All: 0.5 ms/cm

B. Top: Q9 emitter, 0.2 v/cm
Bottom: Q11 emitter, 0.5 v/cm
Both: 0.5 ms/cm

Waveforms in PLAY mode.

Figure 56—Channel Switching and Output, Schematic Diagram and Typical Waveforms (Continued)

quencies and boosted at the high frequencies. Combining the response characteristics of both the amplifier and the delay line, the equalization circuit therefore attenuates the low frequencies and accentuates the high frequencies. Thus the circuit may properly be called a high frequency boost circuit. The amount of boost may be controlled so as to modify the amplitude relationship of carrier to sidebands, in such a manner that the frequency response of the demodulated signal will be properly equalized.

Figure 55 represents the dynamic range of the equalization circuit. As illustrated, the curve is variable over a small range. This range is controlled by the Equalizer potentiometer R24 which controls one of the two inputs of the differential amplifier Q5-Q6.

With the Equalizer potentiometer R24 in the fully counter clockwise position, the curve representing maximum high frequency boost is attained; whereas, with the potentiometer in the fully clockwise position, the curve representing a more nearly flat response is attained. As noted, the control permits a 40% range of adjustment.

The figure 55 also attempts to illustrate the action of the differential amplifier Q5-Q6 by using vectors. The input to the base of Q5 has a phase shifting network in its circuit, while the input to Q6 has an amplitude control in its circuit. With the amplitude of the signal at the same value, the output of the differential amplifier closely approximates the curve A. Curve B approximates the output when the input to Q6 is at a minimum. With the amplitude control set to another position the curve will be anywhere in between these limits.

FM Switch

Transistors Q8, 28 and 29 make up a single pole, double throw switch. The function of this switch is to permit the combining of the two playback channels within the module, thus its output can be combined with the output of the other playback amplifier module in the FM switch module to produce one continuous FM signal containing video and sync information.

Transistor Q29 controls the current flow through transistors Q8 and Q28. Q29 is controlled by a properly timed 4XTW pulse which is produced in the FM switch module. The output at the collector provides the proper potential on the emitters of PNP transistor Q8 and NPN transistor Q28 to permit switching operation.

Refer to figure 56. When the switching pulse at P1-28 is on the positive excursion, Q29 is conducing hard which places −12 volts on resistor R116. Q8 cannot function since it requires a positive return potential on its emitter, but Q28 is turned on and it passes the FM signal on its base. When the switching pulse is on the negative excursion, Q29 is cut off and the emitter of Q8 is returned to +12 volts. Thus the switching pulse turns Q8 and Q28 on and off alternately permitting the two playback channels to combine at the base of transistor Q9.

Output Amplifiers

Refer to figure 56. Transistors Q9 and Q10 form a feedback amplifier. The combined FM signals are amplified and fed to the line driver amplifier Q11 and Q12. This circuit functions the same as Q1 and Q2. The output from this circuit is capacitively coupled to the output pin P1-31 to the FM switcher module.

ADJUSTMENTS

Internal adjustments on each Playback Amplifier module have been carefully set at the factory, and have been sealed with a red or blue sealant indicating a critical factory adjustment which should not be adjusted in the field. If service is required in these areas, contact your RCA field representative.

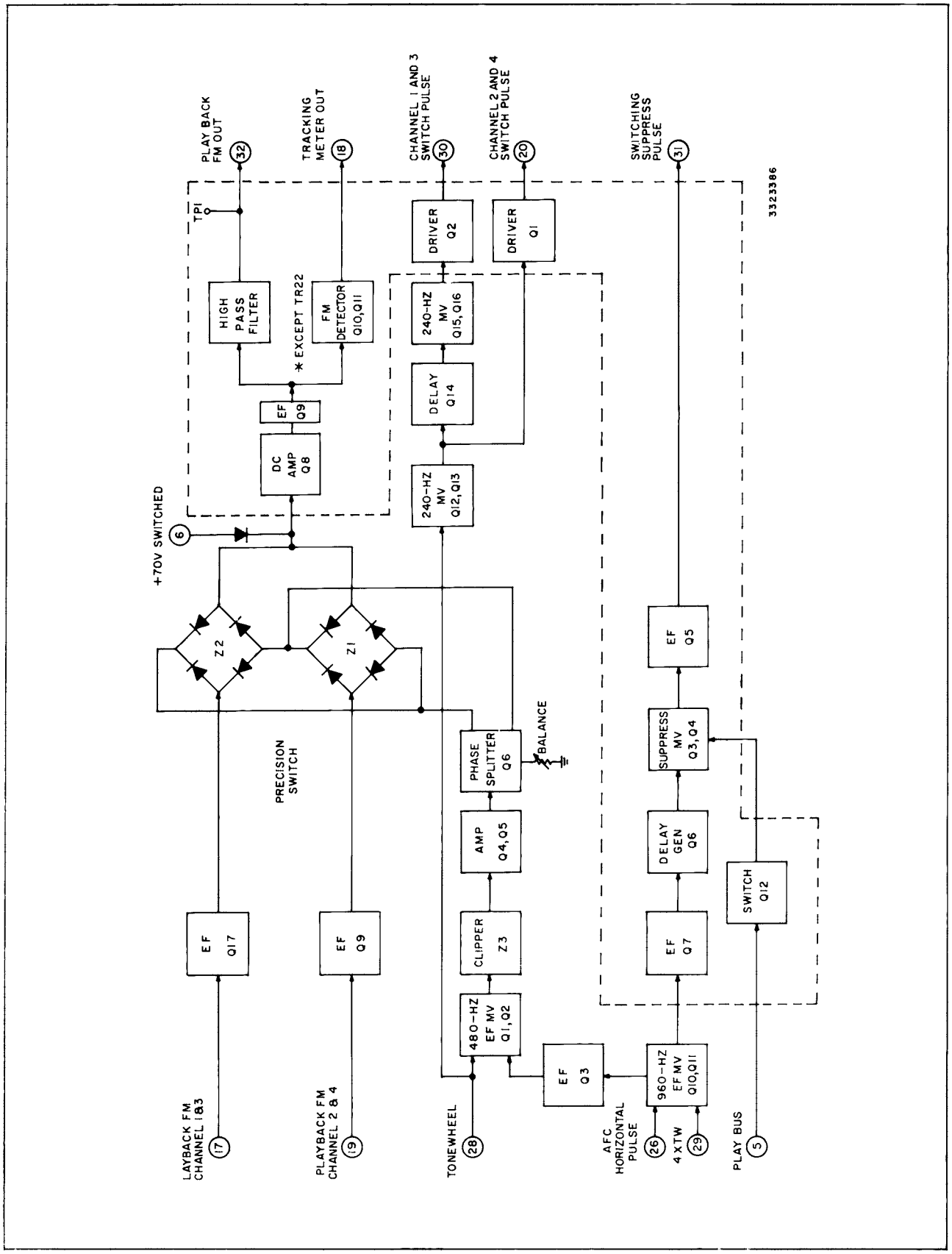


Figure 57—FM Switch Module, Block Diagram

FM SWITCH MODULE

CIRCUIT DESCRIPTION

General

The FM Switch module combines the FM output of the four heads as they sequentially scan the tape during playback. Precision switching places switching transients with respect to video where they are least detrimental. The switching arrangement locates transients during the horizontal sync interval where the transients are later eliminated by substitution with regenerated sync.

Besides combining the playback FM outputs from the four heads, the FM Switch module also generates a suppressor pulse that is used to activate a transient (head-switching) suppression clamp circuit in the Demodulator Output module.

In addition to the above, the FM Switch module provides the coarse switches used in the Playback Amplifier modules.

As seen on the block diagram of the module, figure 57, the functions of the circuits are the same for any high band modified machine covered in this book, only the component symbol numbers are changed. Since, as seen on the chart, the TR-4/50 (serial numbers 4501 to 4600) and the TR-22D tape machines have the same symbol numbers, the descriptive text will cover those machines. It is left to the reader to exchange the symbol numbers for his machine should it be something other than those described.

> NOTE: The FM Switch module operates universally on all television standards. The descriptions that follow are simplified by referring to tonewheel rates only on the basis of 60-Hz systems (240-Hz basic tonewheel frequency). For 50-Hz systems, change the corresponding tonewheel frequency references to 250-Hz.

4X2 Coarse Switch

The coarse switching pulses are generated in the FM Switch module and the actual switching takes place in the Playback Amplifier modules. The odd numbered channels are switched, as are the even numbered channels, so that precise timing is not required between adjacent channels. Thus, the reason for the name—coarse switch. The 4X2 stands for four lines reduced to two lines.

A 240-Hz tonewheel (TW) pulse is used for the control of the 4X2 coarse switch. See the waveform A on timing diagram, figure 58. This tonewheel pulse is generated in the Tonewheel Processor module. Its timing is based on a signal generated in a pickup coil by a notch in the tonewheel as it rotates with the headwheel. Thus, because the tonewheel and headwheel are mechanically connected, the tonewheel pulse has a definite timing relationship with the rotating quadraplex heads. The TW pulse occurs near the center of the active tape scan by head number one. See waveform B. Switching then occurs between input channels in the Playback Amplifier modules during the interval when neither input channel is supplying a tape FM signal.

Switching between channels 2 and 4 is controlled by a monostable multivibrator comprising transistors Q12, Q13. The multivibrator generates a 2080 microsecond pulse (waveform F) that corresponds to one-half the 240-Hz tonewheel period when triggered by the TW pulse. Polarity of the control signal, after being current amplified through driver stage Q1, is such that the channel 2/4 gate, in the Playback Amplifier module, switches to channel 2 before head 2 begins to traverse the tape. (Switching actually occurs at the TW leading edge while head 1 is at the center of the tape.) After head 2 has completed its traverse (2080 microseconds after the initial switch), the channel 2/4 gate switches from channel 2 to channel 4. Thus, disturbances in the desired FM signal are avoided by gating the two inputs signals while both are inactive.

A similar sequence of operation takes place in the channel 1/3 switching. However, the tonewheel pulse cannot be used directly to trigger the control multivibrator Q15, Q16. This would cause switching to occur during the center of the active scan for head 1. The TW pulse is therefore delayed for a time interval corresponding to 90 degrees (1040 microseconds) of rotation of the headwheel by delay generator transistor Q14. See waveform G of figure 58. The trailing edge of the delayed output pulse from Q14 then triggers the 240-Hz multivibrator Q15, Q16 (waveform H) and causes the channel 1/3 gate, in the Playback Amplifier modules, to switch between the intervals when heads 1 and 3 are supplying FM.

2X1 FM Switch

Since the coarse switching has already been accomplished in the Playback Amplifier modules, the precision switching in the FM Switch module combines the FM signals from channel 1 and 3, and channels 2 and 4 to form a continuous playback FM output.

Two diode quads comprise an electronic switch controlled by precisely timed signals developed in the

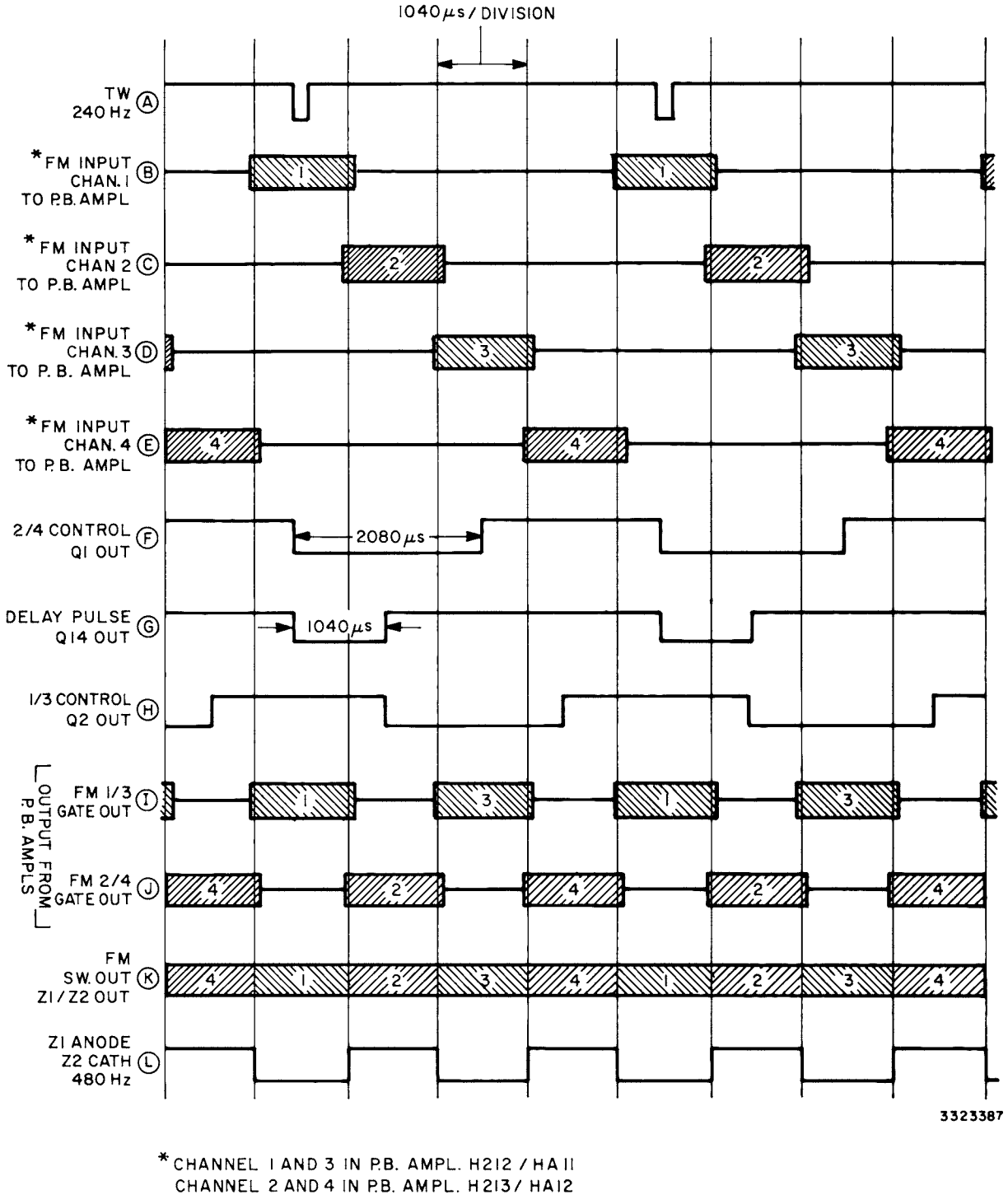


Figure 58—4X2 Coarse Switch Timing Diagram

timing generator circuit of the FM Switch module. One input to the electronic switch is the combined FM from channels 1 and 3 at quad diodes Z2 (waveform D of the timing diagram, figure 59). The second input is the combined FM from channels 2 and 4 at quad diodes Z1 (waveform E).

The outputs of the two quads are connected in parallel to subsequent stages. The control points of the quads are connected in complementary fashion to the push-pull control signals so that the quads select the inputs alternately as a single-pole, double-throw switch. Switching occurs at each polarity reversal of the control signal so that the switch operates at a 960-Hz (4XTW) rate when supplied with a 480-Hz control signal (waveform J).

The 960-Hz switching rate causes the quad diodes to select the channels 1/3 input while head 1 is traversing the tape. The quad diodes then switch to the channels 2/4 input just as head 1 is leaving the tape and head 2 is beginning its scan. As head 2 completes its scan, the quad diodes switch again to the channels 1/3 input to select the output of head 3 as it starts across the tape. When head 3 is nearing the end of its active scan, the quad diodes switch away and select the channels 2/4 input once again as head 4 begins its traverse. Finally, as head 4 nears completion of its scan, the quad diodes return to the channels 1/3 input to begin the sequence again with head 1.

The output from the quad diodes is a continuous FM signal (waveform F) resulting from the sequential selection of playback channels coordinated with the passage of the quadraplex heads across the tape. Because the headwheel rotates at 240 rotations-per-second, a complete cycle in the selection of all four heads must occur at a 240-Hz rate, and selection of individual heads at a 960-Hz rate.

The FM signal in its entirety (waveform F) is fed to the input of a dc stabilized amplifier, Q8 which drives emitter follower Q9. The output of Q9 is coupled to a high pass filter network. This filter network is used to reduce low frequency switching transients below 200 kHz. The output of the filter may be conveniently observed at test point TP1, FM OUT. The output of the filter is also fed to pin 32 where it is supplied to the FM Equalizer module.

When the machine is in the Record or Set Up modes of operation the FM output of the quads is turned off. In the Playback mode the output of the quads is permitted to feed the FM Equalizer. The control for this function is the +70 volt switched which is generated in the Regulator module.

In the TR-3/4/50 machines an FM detector is included so that the FM output can be monitored on a meter.

Timing Generator

The timing generator functions should be thoroughly understood prior to referring to the detailed circuit descriptions.

An AFC horizontal pulse having a repetition rate of 15.75 kHz is generated in the Tape Sync Processor module and enters the FM Switch module via pin 26. See waveform A of figure 59. The pulse is applied to a trigger circuit which sets the 960-H bistable multivibrator using transistors Q10, Q11. The reset trigger for the bistable multivibrator is the 4XTW signal (waveform B) which is developed in the Tonewheel Processor module and enters through pin 29. The Tonewheel Processor module contains the 4XTW DELAY control that permits adjusting the 4XTW pulse to the proper point in the head overlap interval.

The bistable multivibrator (Q10, Q11) is switched to one state by a positive-going transition of the 4XTW signal that is coincident with the beginning of a new head traverse across the tape. The first AFC horizontal sync pulse to occur after the above event then causes the bistable multivibrator to change state again. This results in a negative pulse from transistor Q11 with its leading edge timed by the 4XTW pulse, and its trailing edge timed by the AFC sync pulse (waveform C). The multivibrator is immune to triggering by further AFC sync pulses and is inhibited until it is again reset by the 4XTW trigger as the next head begins crossing the tape.

The negative pulse from transistor Q11 is supplied at a 960-Hz rate to emitter follower Q3. The positive-going transition (trailing edge) from Q3 triggers bistable multivibrator Q1, Q2 which operates as a two-to-one frequency divider. The square wave output from Q1/Q2 is at a 480-Hz rate (waveform G) and is clipped by shunt limiter Z3.

The signal is then supplied to an amplifier and phase splitter where push-pull control signals (waveforms H and J) are developed to drive the video channel precision switch (Z1, Z2). The output of the quads is a continuous FM signal (waveform F) from inputs to the quads from channels 1/3 and channels 2/4. Proper phasing of the bistable multivibrator Q1/Q2 is assured by introducing a TW pulse (waveform K) to reset it in the event that the phase is incorrect.

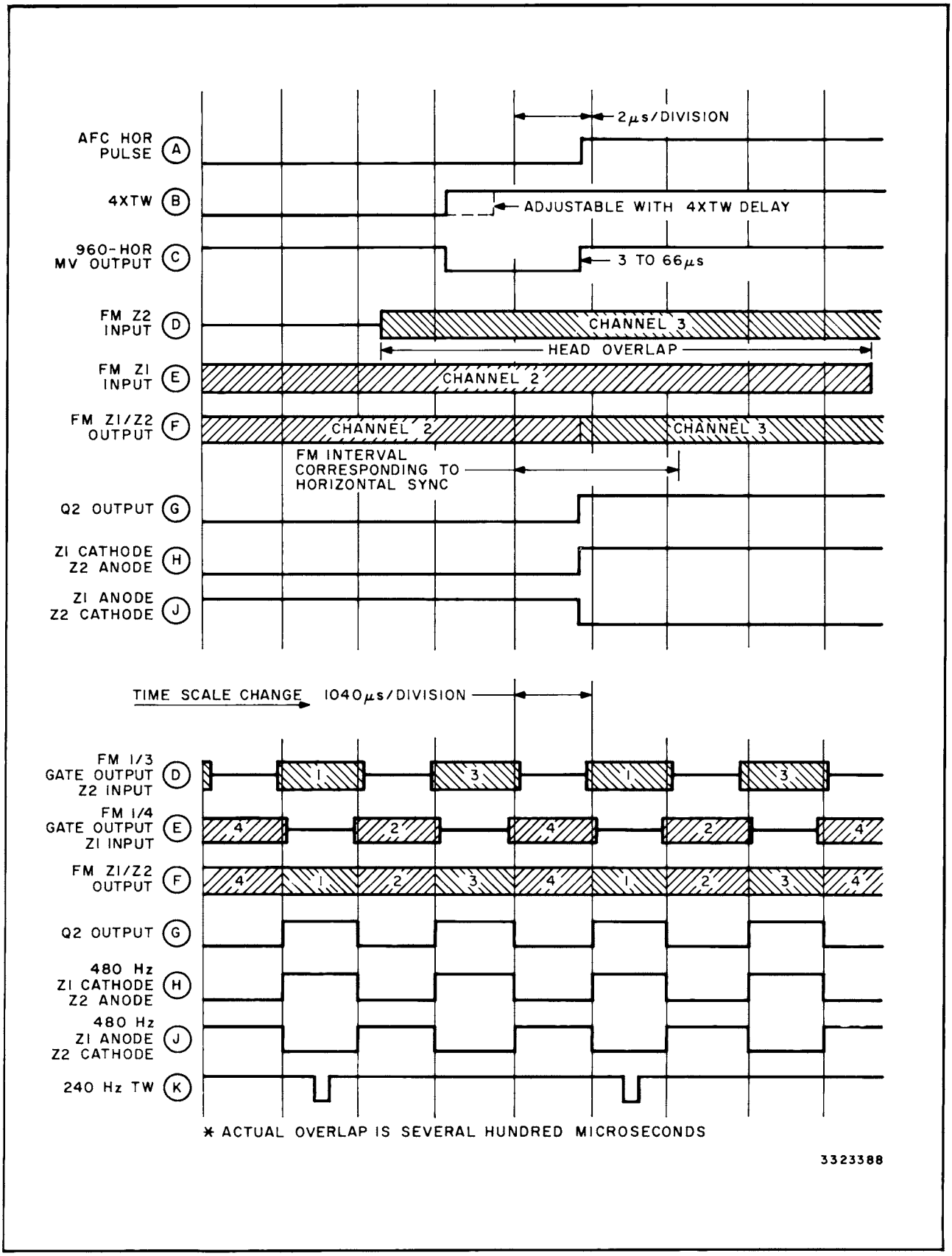


Figure 59—2X1 FM Switch Timing Diagram

NOTE: Head overlap of adjacent channels is several hundred microseconds, but is shown greatly reduced in the timing diagrams to simplify illustration of the various functions.

Head Switching Pulse Suppressor Generator

A 3 usec pulse derived from the head switching multivibrator, Q10-Q11, is also generated in the FM Switcher module and fed to the sync separator in the Demodulator Output module where it is used to suppress the transient due to the electronic switching from one head output to the next. The pulse is delayed approximately 1.5 usec by Q6 to account for the delay of the demodulation system. The pulse width is established by multivibrator, Q3-Q4. The output is clamped out by Q12 except when activated by the Play bus.

240-Hz and Delayed 240-Hz Multivibrator

Both of these multivibrators as shown on figure 60 are of the monostable type and generate a 2080-microsecond pulse when triggered. After generation of a pulse is completed, the circuit returns to a stable state with transistor Q12 saturated while Q13 is cut off in the 240-Hz multivibrator.

The negative-going tonewheel pulse supplied through pin 28 is coupled through a trigger network. The negative trigger caused Q13 to conduct and its collector potential becomes more positive due to the voltage drop across the collector resistor. The positive-going change is coupled to the base of Q12 to cut off that transistor. With Q12 cut off, its collector potential goes more negative and a portion of this negative voltage is transferred to the base of Q13 to reinforce the negative trigger pulse (tonewheel pulse).

The 240-Hz multivibrator remains in the unstable state until capacitor C29 charges toward −20 volts through resistor R67, for a period of 2080 microseconds. After this time, the potential on the base of Q12 becomes sufficiently negative to cause that transistor to conduct, thus returning the multivibrator to its quiescent state. The time interval of 2080 microseconds is equal to one-half of the 250-Hz period. It is a compromise period that accommodates both domestic and international (250-Hz) machines. See waveform F of figure 58.

During the time that the 240-Hz multivibrator is in the unstable state, the negative pulse on the collector

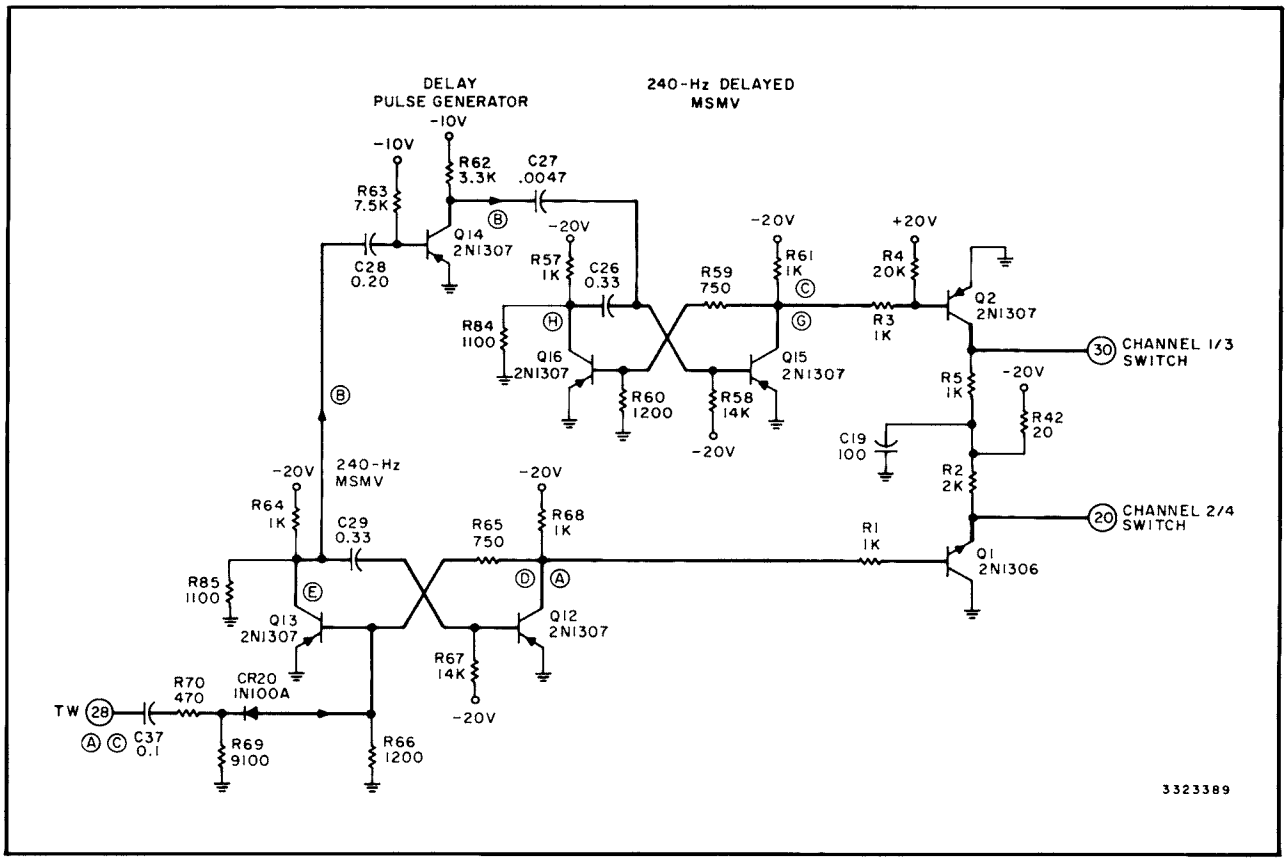
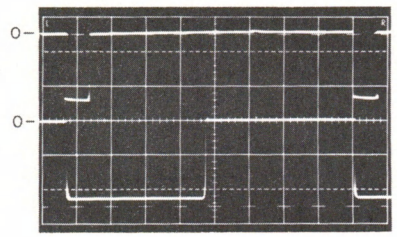
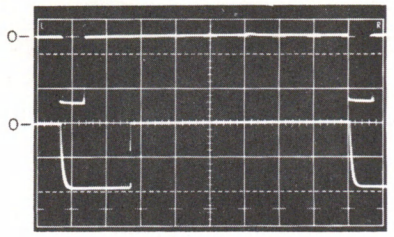


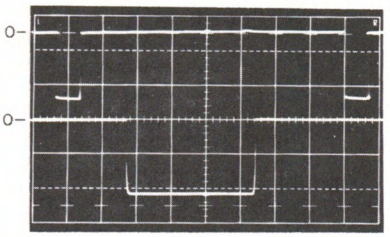
Figure 60—240-Hz Multivibrators, Schematic Diagram and Typical Waveforms



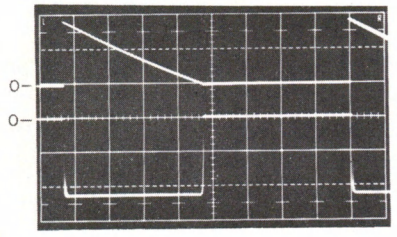
A. Top: P1 pin 28
Bottom: Q12 collector
Both: 5 v/cm, .5 ms/cm



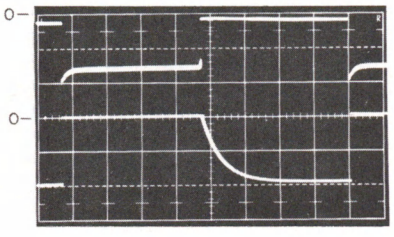
B. Top: Q13 collector, 5 v/cm
Bottom: Q14 collector, 10 v/cm
Both: .5 ms/cm



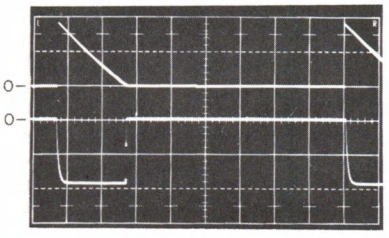
C. Top: P1 pin 28
Bottom: Q15 collector
Both: 5 v/cm, .5 ms/cm



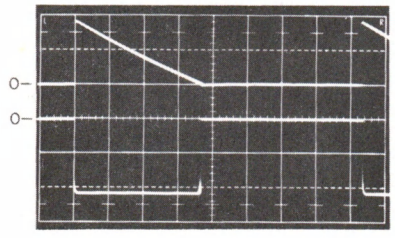
D. Top: Q12 base
Bottom: Q12 collector
Both: 5 v/cm, .5 ms/cm



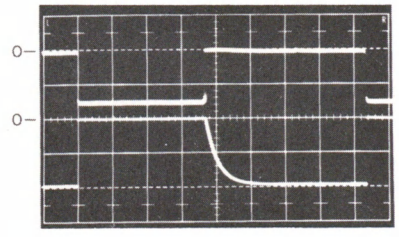
E. Top: Q13 base, .2 v/cm
Bottom: Q13 collector, 5 v/cm
Both: .5 ms/cm



F. Top: Q14 base, 5 v/cm
Bottom: Q14 collector, 10 v/cm
Both: .5 ms/cm



G. Top: Q15 base
Bottom: Q15 collector
Both: 5 v/cm, .5 ms/cm



H. Top: Q16 base, .2 v/cm
Bottom: Q16 collector, 5 v/cm
Both: .5 ms/cm

All waveforms in PLAY or STANDBY mode.

Figure 60—240-Hz Multivibrators, Schematic Diagram and Typical Waveforms (Continued)

of Q12 is applied to the output driver Q1 and then supplied to the channels 2/4 gate in the Playback Amplifier module via pin 20. At the same time the positive pulse produced on the collector of Q13 is coupled through capacitor C28 to the base of delay pulse generator Q14.

Normally, transistor Q14 is conducting to saturation. The negative portion of the drive signal causes transistor Q14 to conduct still harder, but when the positive-going transition occurs, it is coupled to the base of Q14, cutting off the transistor. Capacitor C28 then charges toward minus 10 volts. The transistor remains cut off for a period of 1040 microseconds as determined by the charge rate of capacitor C28 through resistor R63. After the elapse of 1040 microseconds, the base of Q14 becomes sufficiently negative to cause the transistor to conduct to full saturation again. The resulting 1040-microsecond negative pulse at the collector of Q14 is the delay period at which the 240-Hz delayed multivibrator (Q15, Q16) is held in quiescence after the 240-Hz multivibrator has been triggered.

The negative delay pulse from the collector of Q14 is coupled through differentiator-capacitor C27 and is applied to the base of Q15. In the quiescent state, transistor Q16 is cut off while Q15 is in saturation. However, at the completion of the delay period, the trailing edge of the delay pulse cuts off transistor Q15. The multivibrator now reverses its state and remains thus for a period of 2080 microseconds, as

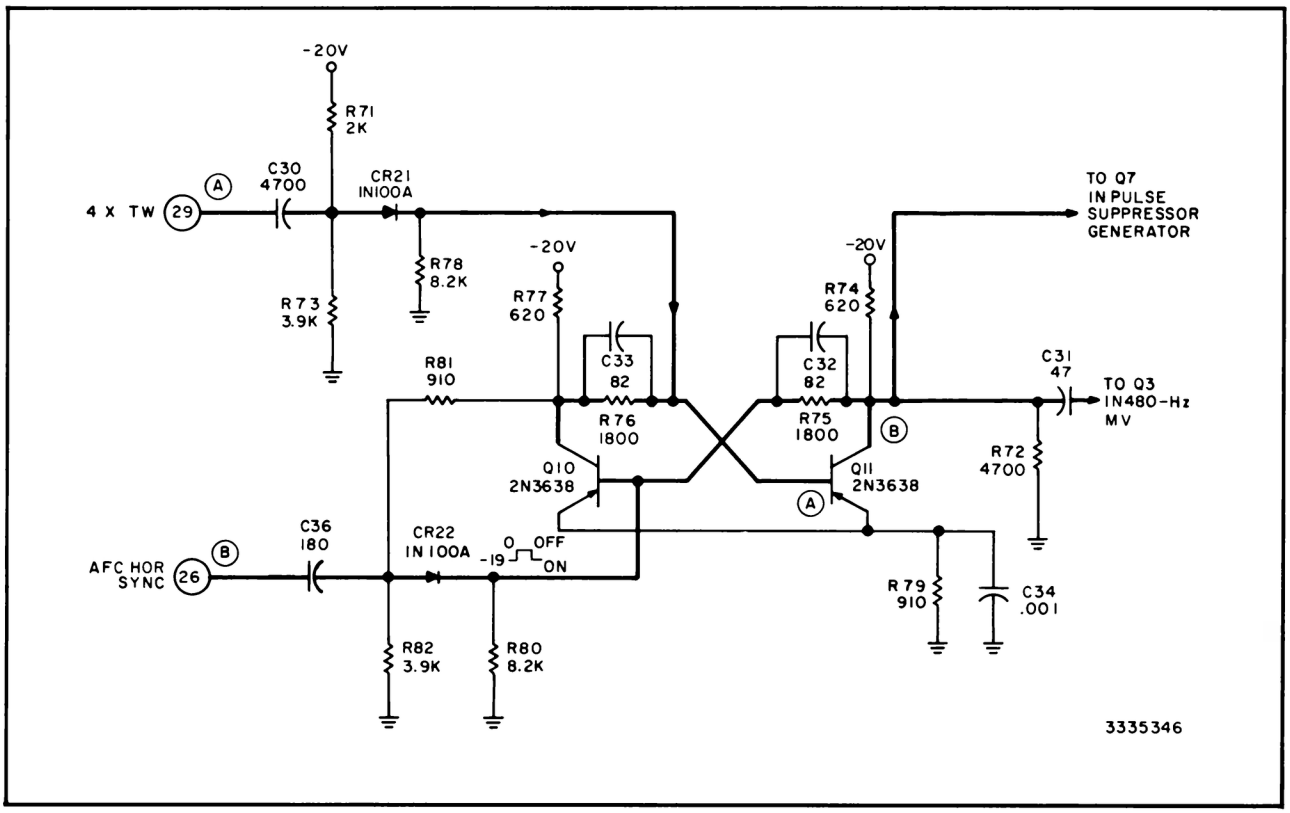
determined by the time constant of capacitor C26 and resistor R58. This delayed negative pulse at the collector of Q15 is applied to the output driver Q2 to the channels 1/3 gate in the Playback Amplifier module via pin 30.

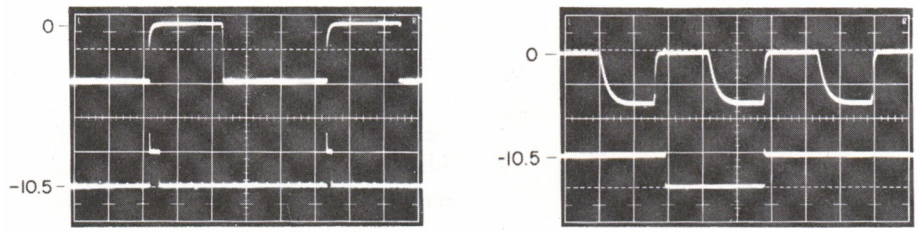
960-Hz Bistable Multivibrator

The 960-Hz bistable multivibrator (Q10, Q11) generates pulses that are eventually used to control the precision switch, diode quads (Z1, Z2). Refer to figure 61. The application of these pulses require that their rate be halved and that they be clipped prior to usage.

Transistors Q10 and Q11 form a bistable multivibrator (flip-flop) that remains in the state in which it was last triggered. Pulses at a 4XTW rate are supplied from the Tonewheel Processor module through pin 29 and coupled through differentiator capacitor C30. Positive transitions of these pulses forward bias diode CR21 and pass through the diode to the base of Q11.

With reception of a positive level, transistor Q11 cuts off. The collector becomes more negative and a portion of this negative level is transferred through resistor R75 to the base of Q10. The latter transistor now conducts to saturation and supplies a more posi-



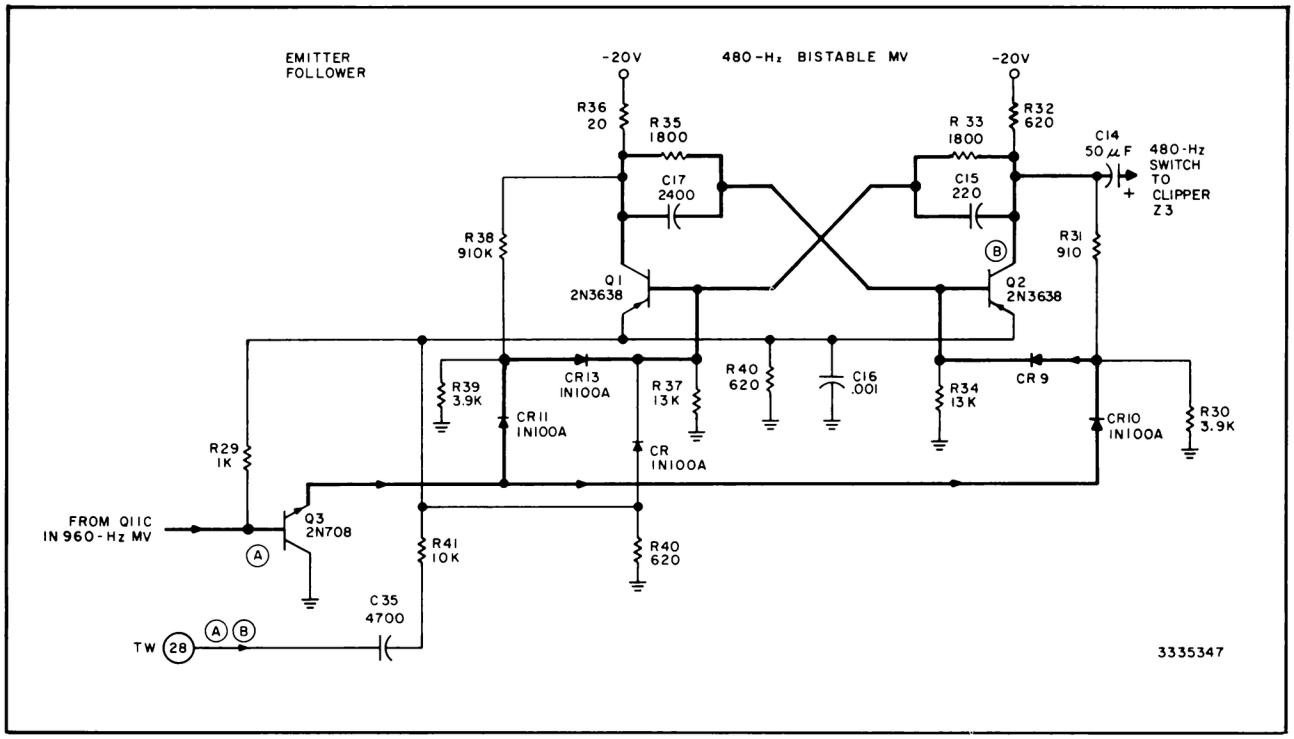


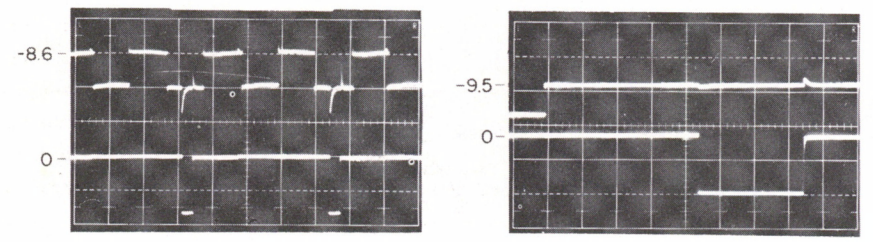
A. Top: P1 pin 29, 5 v/cm
Bottom: Q11 base, 2 v/cm
Both: 0.2 ms/cm

B. Top: P1 pin 26, 10 v/cm
Bottom: Q11 collector, 5 v/cm
Both: 20 μs/cm

Waveforms in PLAY mode.

Figure 61—960-Hz Bistable Multivibrator, Schematic Diagram and Typical Waveforms





A. Top: Q3 base, 0.2 v/cm
Bottom: P1 pin 28, 5 v/cm
Both: 1 ms/cm

B. Top: Q2 collector
Bottom: P1 pin 28
Both: 0.1 ms/cm

Waveforms in PLAY mode.

Figure 62—480-Hz Bistable Multivibrator, Schematic Diagram and Typical Waveforms

tive voltage from its collector through resistor R76 to the base of Q11 to hold that transistor cut off. The multivibrator is now set in a condition that is prepared for reception of the first AFC horizontal sync pulse, which will reverse the state of the multivibrator.

AFC horizontal sync pulses are supplied continuously at the horizontal rate through pin 26. Reception of each negative-going sync pulse produces negative and positive spikes at the junction of C36 and R82-R81. The positive-going transitions forward bias CR22 and pass through. The first positive pulse to pass through diode CR22 after the multivibrator is in a set condition, reverses the condition of the multivibrator. Thus the multivibrator has been in a set state at the time beginning with the positive transition of the 4XTW pulse until the beginning of the first AFC horizontal sync pulse.

This period of time is variable because it depends on the timing that follows a 4XTW pulse with respect to video horizontal timing. Further AFC horizontal sync pulses do not affect the condition of the multivibrator until it has been reset by reception of a positive-going 4XTW pulse.

The negative pulse from the collector of Q11 is supplied to transistor Q7 in the pulse suppressor generator circuit. The positive-going transition of the same pulse is coupled to the 480-Hz multivibrator (Q1, Q2) via emitter follower Q3.

480-Hz Bistable Multivibrator

This circuit gates the switch pulses with pulses supplied from the 960-Hz multivibrator (Q10, Q11) to provide precise switching intervals for the FM switch. Precisely timed pulses thus obtained at a 960-Hz rate, trigger the 480-Hz multivibrator which generates the switch control signal. Refer to figure 62.

Input from the 960-Hz bistable multivibrator (Q11) is coupled directly to the base of emitter follower Q3. The transistor provides a low impedance source for the bistable multivibrator that follows.

The input pulse supplied to transistor Q3 is negative-going and at a 960-Hz rate. The leading edge of the pulse is timed by the 4XTW pulse and the positive-going trailing edge by the AFC horizontal sync pulse. The positive transition of this pulse causes transistor Q3 to conduct and supply a positive-going pulse to the multivibrator.

Transistors Q1 and Q2 form a bistable multivibrator (flip-flop) that changes state each time a trigger pulse from Q3 is supplied. The multivibrator is phased by the TW pulse supplied from the Tonewheel Processor module with a positive pulse through pin 28 and diode CR12. The TW pulse sets the multivibrator so that transistor Q2 is conducting and supplying a positive level while head 1 is sweeping on the tape. Each subsequent trigger pulse supplied from Q3 then triggers the multivibrator to cause it to change state with the pulse. Thus, the output from the collector of Q2 is positive for one pulse, negative for the next pulse, then returns to positive for the succeeding pulse. This results in one complete cycle for each two pulses of input, thereby providing an output rate of one-half the input rate. The collector output from Q2 is coupled through capacitor C14 to the clipper (Z3) in the switch driver circuit that follows.

Switch Driver and Switch

Final switching for the FM channels occurs in these circuits which results in the two video FM channels being combined to form a single channel of FM. Pulses at a 480-Hz rate are supplied through resistor R11 and clipped by the diodes in clipper Z3 to remove transients that may be present in the multivibrator output signal. The 480-Hz square waves are then coupled through capacitor C12 to the base of Q4. See figure 63.

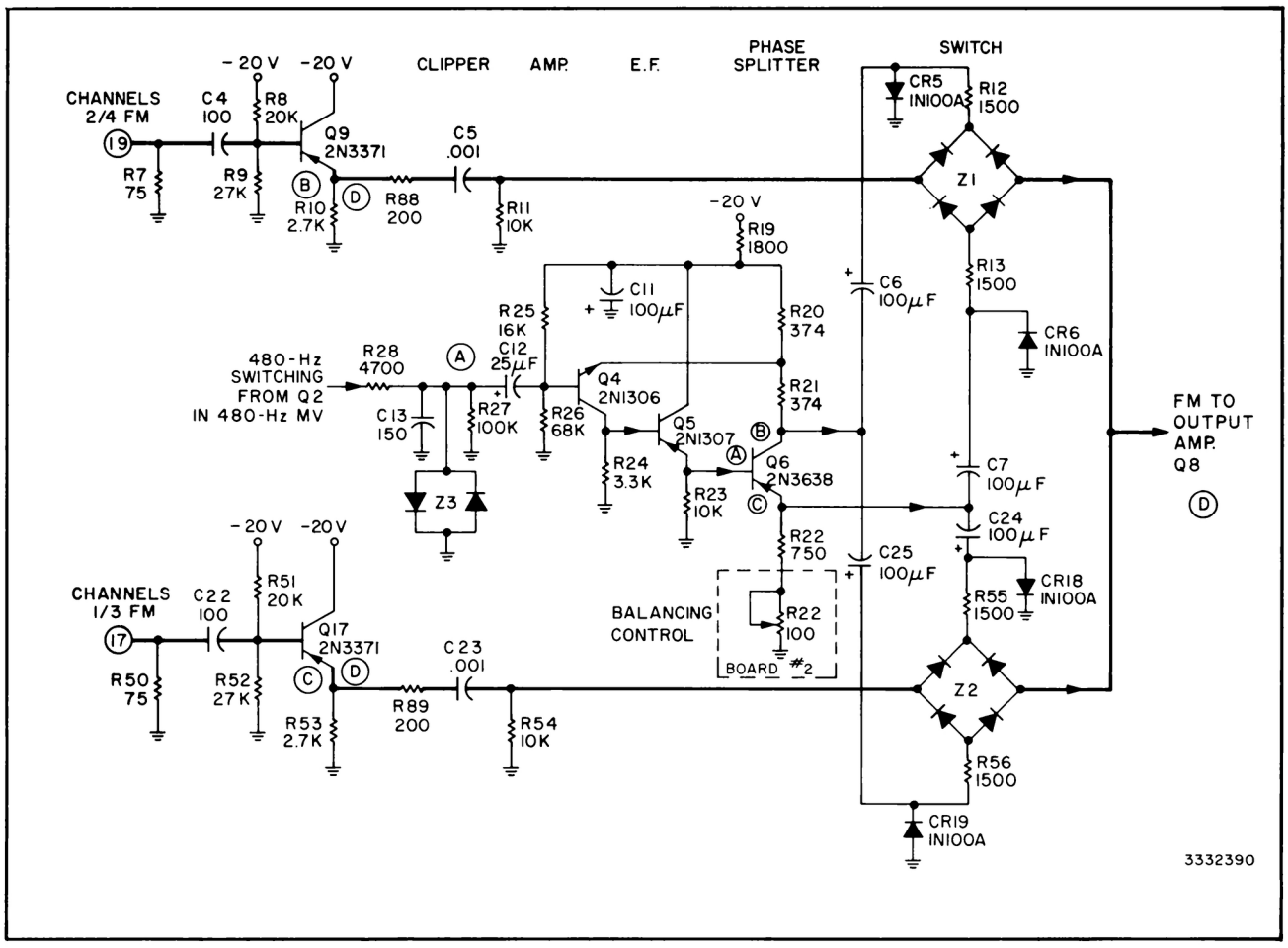
The inverted output from Q4 is coupled through emitter follower Q5, which supplies the signal to the base of Q6 without further inversion. Transistor Q6 is a phase splitter that supplies an output from its emitter in the same phase supplied from the collector of Q4. The collector output of Q6 is of opposite phase which results in square-wave output signals that are equal but of opposite phase. A portion of the collector output from Q6 is fed back through resistor R21 to the emitter of Q4 to maintain stability. Potentiometer R22 on board No. 2 is adjusted to provide symmetry between the positive and negative excursions of the square waves so that the emitter and collector outputs from Q6 are equal.

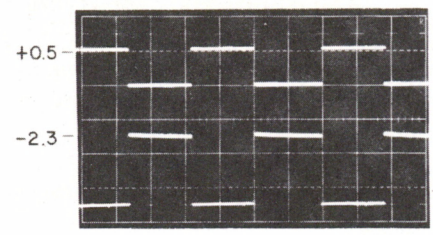
Quad diodes Z1 and Z2 provide switching required to combine channels 2/4 with channels 1/3. Each quad diode is alternately switched on and off once at a 480-Hz rate so that quad Z2 is forward biased when channel 1 FM is present on its input, but is cut off upon completion of head 1 sweep across the tape. At that same period, quad Z1 is cut off, but is forward biased upon completion of head 1 sweep, and remains on for the period of time required for head 2 sweep. Thus, the quad diodes continue to switch on and off alternately to accommodate their respective input signals.

At the time that the square-wave input to the base of Q6 is negative, its collector output is positive and its emitter is negative. The positive-going output from the collector is coupled through capacitors C6 and C25 to each quad. The positive pulse through capacitor C25 passes through resistor R56 and forward biases the anodes input to quad diode Z2. However, the same positive pulse also is coupled through capacitor C6 and is clamped to a slightly positive level with diode CR5. This positive potential is sufficient to reverse-bias the cathodes input to quad Z1 and reverse-bias that side of the bridge.

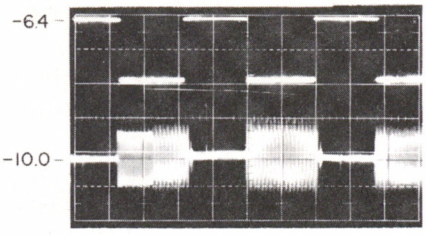
Meanwhile, the negative level from the emitter of Q6 is coupled through capacitors C7 and C24. This negative level passes through resistor R55 to forward bias the cathodes input to quad Z2, thereby completely forward biasing the bridge and allowing channel 1 (or channel 3) FM to pass through the bridge. At the same time, the same negative level from the emitter of Q6 is coupled through capacitor C7 and resistor R13 to the anodes input to quad Z1. This completes the cutoff biasing of quad Z1 thereby blocking any input to that bridge.

The positive half of the 480-Hz square wave to the base of Q6 reverses the entire operation of the quad diodes to cause quad Z1 to be forward biased while Z2 is cut off. Thus, channel 2 (or channel 4) information passes through quad diode Z1 but quad diode Z2 is cut off.

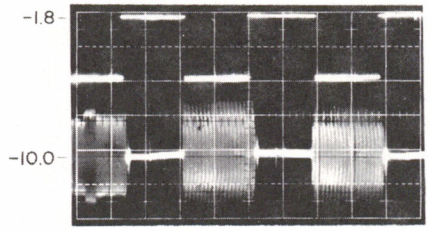




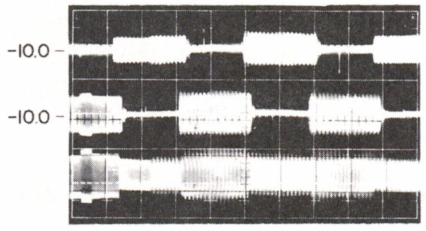
A. Top: R28/C12
Bottom: Q6 base
Both: 1 v/cm, 0.5 ms/cm



B. Top: Q6 collector, 1 v/cm
Bottom: Q9 emitter, 0.2 v/cm
Both: 0.5 ms/cm



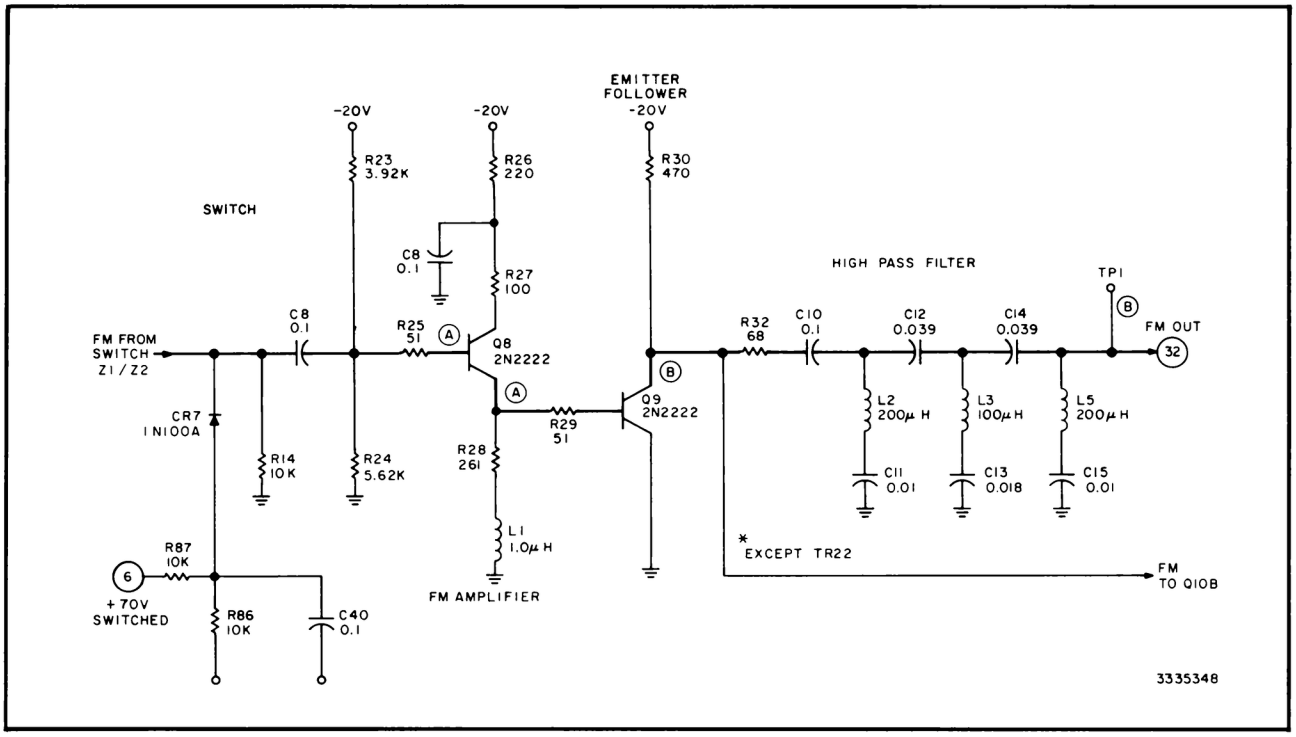
C. Top: Q6 emitter, 1 v/cm
Bottom: Q17 emitter, 0.2 v/cm
Both: 0.5 ms/cm

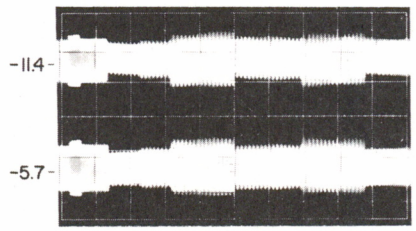


D. Top: Q9 emitter, 0.5 v/cm
Middle: Q17 emitter, 0.5 v/cm
Bottom: Q8 base, 0.2 v/cm
All: 0.5 ms/cm

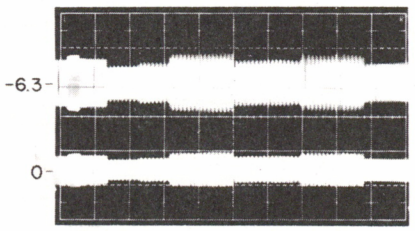
Waveforms in PLAY mode.

Figure 63—Switch Driver and Switch, Schematic Diagram and Typical Waveforms





A. Top: Q8 base, 0.2 v/cm
Bottom: Q8 collector, 0.5 v/cm
Both: 0.5 ms/cm



B. Top: Q9 emitter
Bottom: P1 pin 32
Both: 0.5 ms/cm

Waveforms in PLAY mode.

Figure 64—Line Driver and Filter, Schematic Diagram and Typical Waveforms

Because the quad diodes are conducting in an alternate fashion, their combined outputs present information from the four heads in sequential form. The FM signal is then supplied to the line driver for further processing prior to leaving the module.

FM from channels 2 and 4 is supplied to the FM Switch module from the Playback Amplifier module via pin 19. FM from channels 1 and 3 is supplied to the FM Switcher module from the Playback Amplifier module via pin 17. The signals are passed through emitter followers, Q9 and Q17, and coupled to the switches through capacitors C5 and C23.

Line Driver and Filter

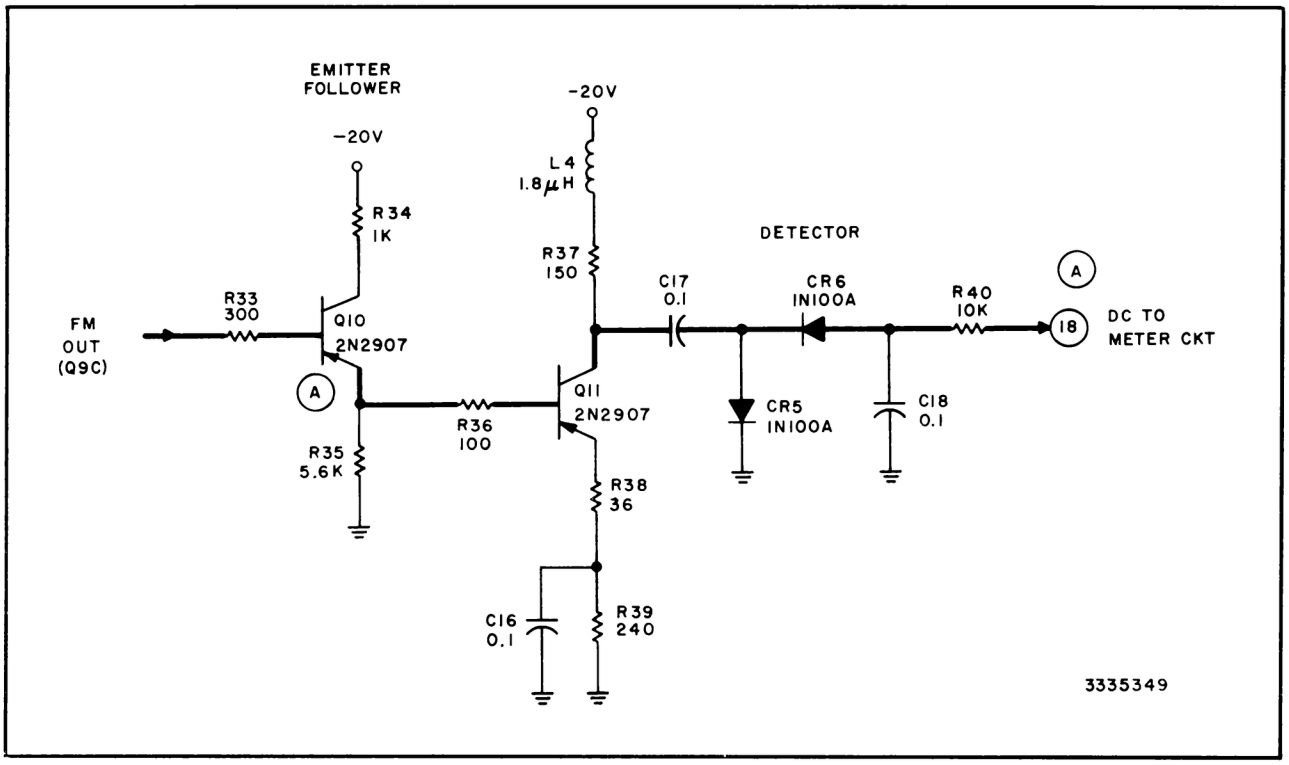
FM is amplified and filtered through this circuit, then supplied from the module. Diode switching is included to prevent crosstalk or other interference from being fed into the playback during RECORD operation. See figure 64.

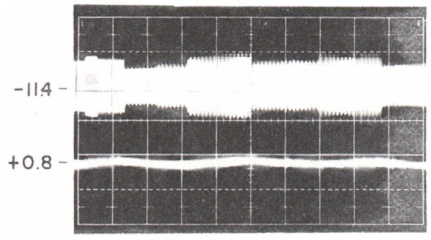
Capacitor C8 couples the input FM through resistor R24 and to the base of Q8 for amplification. Resistor R14 on the input line provides ground reference for the diode quads (Z1 and Z2). Coil L1 in the collector of Q8 provides high frequency stability. Amplified FM from the collector of Q8 is coupled directly to the base of emitter follower Q9.

The emitter output from Q9 supplies FM to a highpass filter. Resistor R32 terminates the sending end of the filter. Response of the highpass filter is such that very low frequencies that are caused by switching, cannot pass through. However, frequencies present in the FM signal are permitted to pass. After filtering, the FM output signal leaves the module via pin 32 and is supplied to the FM Equalizer module.

When the machine is in the Record or Set Up modes of operation, the FM output of the quads is turned off. The circuit that controls the on-off functioning of the quads is composed of CR7, C40 (C10 on TR-3/4/50), R86 and R87 (R26 and R27 on TR-3/4/50). In the Record of Set Up modes, the +70 volts switched signal is on in the Regulator module. This develops a positive bias across R87 (R27). The positive potential is sufficient to offset the reverse bias applied to CR7 by the negative potential developed across R86 (R26) from the −20 volt bus. With the reverse bias overcome, CR7 conducts and any output from the quads passes to ac ground through the path provided by C40 (C10).

When the machine is in the Play mode, the +70 volts is switched off and CR7 will be cut off due to the reverse bias applied to it from the −20 volt bus through R86 (R26). Thus, in this mode, the signal appearing at the output of the quads will follow the path going to Q8, the FM Amplifier.





A. Top: Q10 emitter, 0.5 v/cm
Bottom: P1 pin 18, 2 v/cm
Both: 0.5 ms/cm
PLAY mode

Figure 65—FM Detector for TR-3/4/50 Only, Schematic Diagram and Typical Waveforms

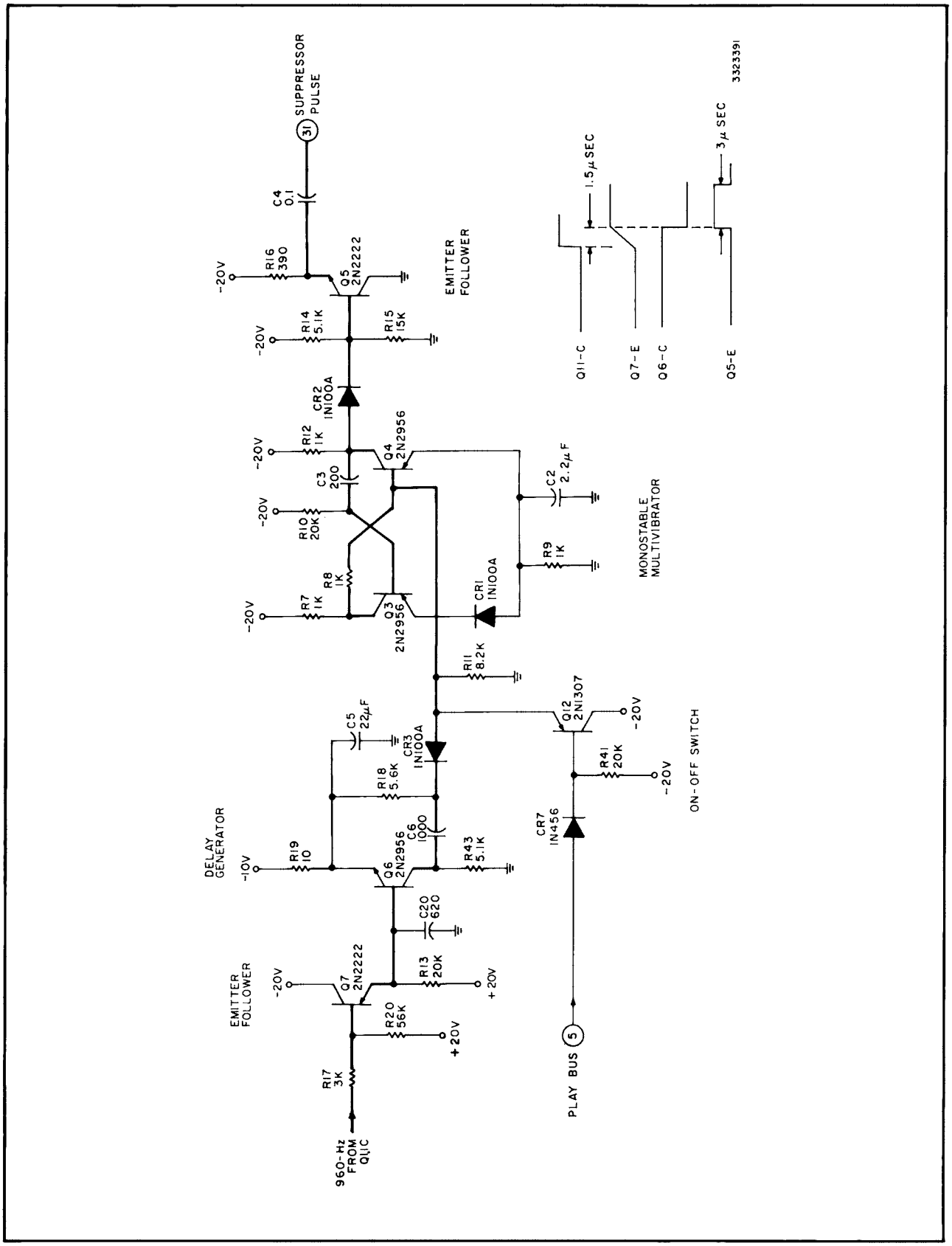


Figure 66—Head Switching Pulse Suppressor Generator, Schematic Diagram and Typical Waveforms

FM Detector (TR-3/4/50 Only)

The purpose of the FM detector circuit, shown on figure 65, is to furnish a rectified signal to the FM meter that represents the signal strength of the playback signal from the tape.

A portion of the FM output before passing through the high-pass filter is fed to emitter follower Q10. Q10 isolates the effects of the FM detector from the high-pass filter. The signal is then applied to the base of the FM detector driver, transistor Q11. The driver amplifies the signal and supplies the output at the collector to the peak-to-peak detector CR5 and CR6.

Dc from the detector circuit is fed to the FM meter via pin 18.

Head Switching Pulse Suppressor Generator

This circuit shown in figure 66 provides pulses that are derived from head switching. The output from Q11-C is coupled to emitter follower, Q7. When the signal goes negative, Q7 conducts, charging C20 to the negative potential of the signal applied to the base of Q7. When the signal goes positive, Q7, cuts off, and C20 charges through R13 toward +20 volts. When the charge on C20 reaches −10 volts, the potential on the emitter of Q6, Q6 will turn on. The turn on time of Q6 will thus be delayed from the input positive going edge by the time taken for C20 to charge (approximately 1.5 usec).

As Q6 turns on, its collector potential falls from 0 to −10 volts. This delayed negative going edge is used to trigger the suppressor pulse multivibrator, Q3-Q4. The suppressor pulse multivibrator however, is prevented from operating unless Q12 is cut off by application of the Play bus to its base. Therefore, the suppressor pulse output is coupled to emitter follower, Q5, only in the Play mode. Q5 provides a low impedance drive for the signal output to the sync separator in the Demodulator Output module.

The output suppressor pulse is a narrow pulse delayed slightly from the actual FM Switch pulse to account for the Demodulator delay of the Video signal. Since the FM Switch pulse and the Suppressor pulse are derived from AFC Horizontal, their timing will shift together. When the timing is set properly for switching to fall in the first 1/3 of the demodulated sync pulse, the supperssor pulse will also fall within sync and will completely enclose switching. It is used in the sync separator to clamp out discontinuities in the output separated sync.

ADJUSTMENT

The only adjustment in the FM Switch module is the Balance potentiometer located on the second board. Its purpose is to keep the quad drive pulse of equal amplitude.

1. Place an oscilloscope probe on the output of either quad (yellow dot).

2. Put the machine into Standby in order to supply the pulse drives to the module.

3. With the oscilloscope preamplifier on a high gain, adjust the balance potentiometer until the line presentation is flat. If the adjustment is off, the oscilloscope presentation will have steps in it. The width of the steps equal to a playback of one head.

FM EQUALIZER MODULE

General

The FM Equalizer module shown on figure 67, performs three basic and separate functions:

1. Provides equalization of the tape FM signal.

2. Provides a detected display signal for the CRO monitor during normal playback and when operating in the E-E mode.

3. Provides an improved signal-to-noise ratio of the playback FM signal prior to demodulation by passing the signal through filters in the module.

The FM Equalizer section performs two functions. Primarily, it provides additional equalization of the tape FM signal. This equalization is very similar to the equalization performed in the individual Playback Amplifier modules, except that in this module the head outputs have been previously combined in the FM Switch module. After equalization, the tape FM signal is supplied to the FM Filter section of this module or to the FM Reference module when the WHITE INSERT button on the Record Switch module is depressed.

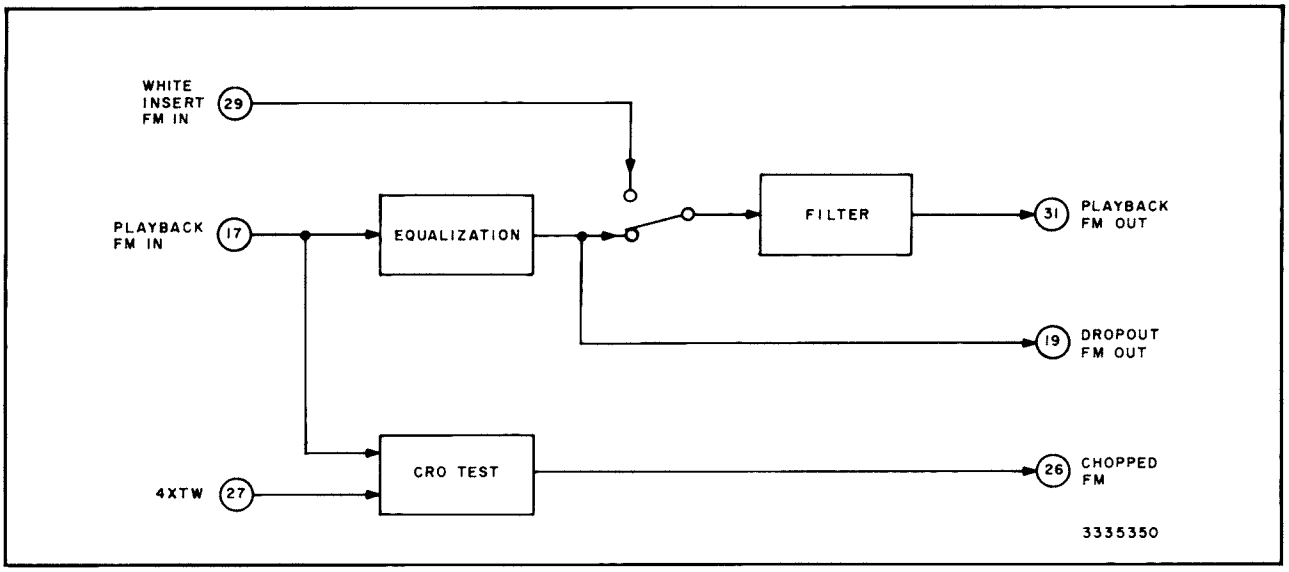


Figure 67—FM Equalizer Module, Block Diagram

The secondary function of this section is to provide a detected display signal for the CRO during normal playback. The detected display is observed by depressing the SW OUT button on the CRO monitor.

The FM Filter section is used to improve the signal-to-noise ratio of the playback FM signal prior to demodulation. Signal recovered from tape has a frequency response characteristic as shown by the curve S1 in figure 68-A. Noise accompanying the signal has a peaked characteristic as denoted by the curve N1.

In the tape machine, the high frequency components of the FM signal are boosted to equalize the frequency response of the signal. This produces a flat frequency response characteristic as denoted by curve S2 of figure 68-A. However, this causes still greater peaking of high frequency noise components (curve N2) and results in a poor signal-to-noise ratio at high frequencies. The FM Filter section presents an attenuation characteristic that increases linearly with frequency until it reaches a null point. Above the null, the filter has no transmission.

The FM Filter section contains a linear rolloff filter which operates on the principle that for a given deviation, video output from an FM demodulator depends only on the ratio of *total* sideband energy to carrier energy. Thus, if both the carrier amplitude and sideband (both upper and lower) amplitudes are reduced by one-half, there will be no change in the demodulated signal. Similarly, if the carrier amplitude is held constant, the upper sideband can be completely eliminated provided that the lower sideband amplitude is doubled. In either condition, the ratio of carrier energy versus *total* sideband energy is unchanged, and therefore the demodulated signal remains unchanged. The linear rolloff filter produces a similar neutral effect on the FM signal.

Figure 68-B shows the spectrum of a typical FM signal encountered during video recording. It consists of a discrete carrier (f_C) and two sidebands. (Although other sidebands may be present, they are not significant in this discussion.) Each of the sidebands (f_L and f_H) is separated from the carrier by a frequency corresponding to the original video modulating frequency. Relative amplitudes have been assigned to the spectrum components to facilitate this explanation. In this example, the total energy contained in the sidebands is one-half the carrier amplitude.

Figure 68-C illustrates an ideal linear rolloff attenuation curve and its effect on the FM spectrum components. Although all components are reduced in amplitude in varying degrees, note that the *total* energy in the upper and lower sidebands (0.05 unit plus 0.15 unit) remains one-half the carrier energy (0.4 unit). Thus, while all amplitudes in the FM spectrum have been modified, the critical sideband/carrier ratio remains unchanged, and demodulated video from this type system would be indistinguishable from a system not having a linear rolloff filter.

A different condition results, however, when noise from the tape is included, as shown in figure 68-D. Because the filter attenuation is greatest in the frequency range in which the noise is at a peak, high-frequency noise components are diminished more rapidly than FM carrier and sidebands. In addition,

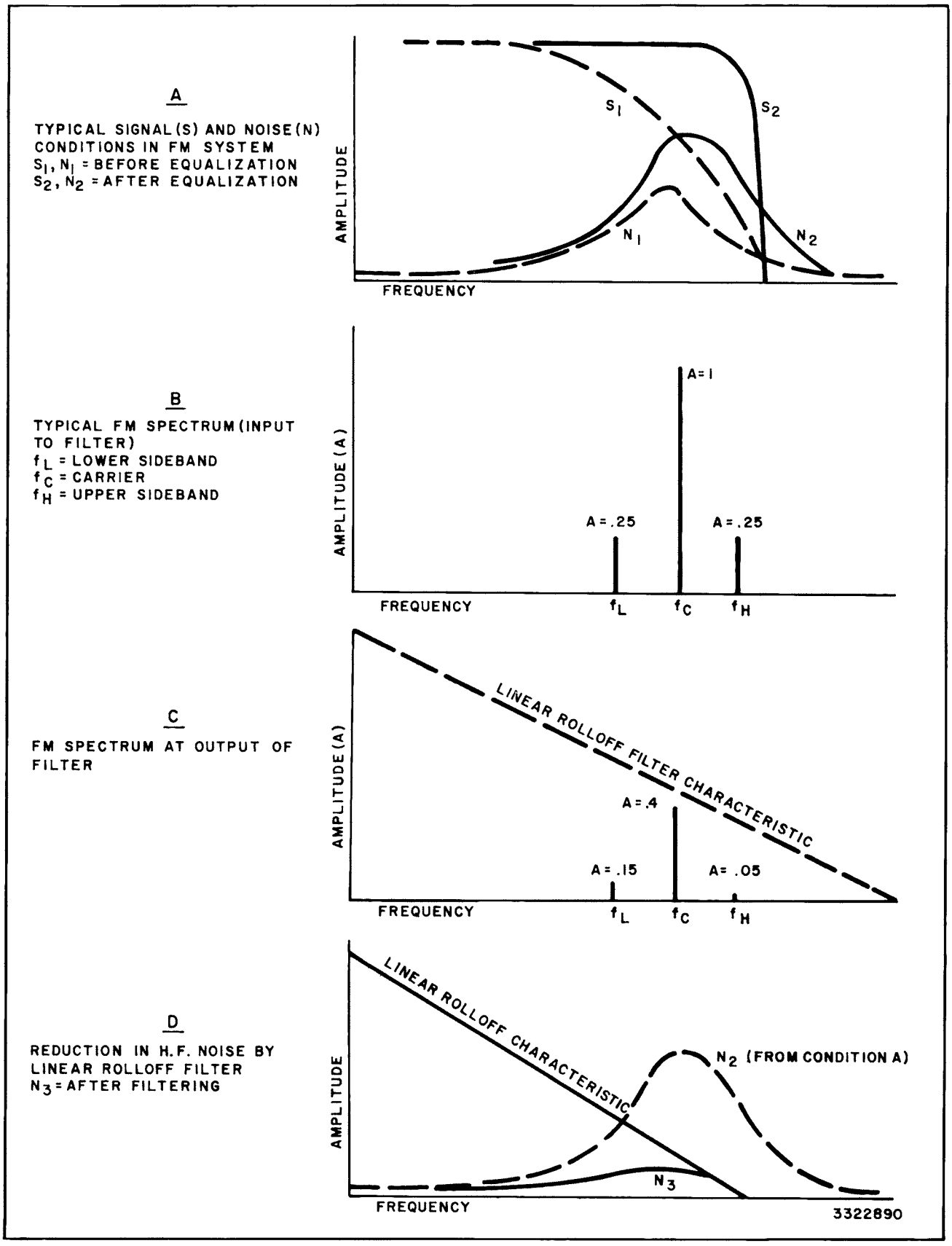


Figure 68—Conditions of FM Recording

all noise above the filter null frequency is completely eliminated. This improved noise characteristic is depicted by N3 in figure 68-D. The final result is that the linear rolloff reduces noise without influencing the signal and therefore may be used in the FM system to improve signal-to-noise ratio and enhance the quality of the playback video.

CIRCUIT DESCRIPTION—FM EQUALIZER SECTION

General

FM input from the FM Switch module is coupled through emitter follower Q20 to a lowpass filter with a three-dB null point at 30 MHz. Filtered FM is then coupled through emitter follower Q19 to the series amplifier using transistors Q17 and Q18. See figure 69.

Series amplifier Q17/Q18 drives the FM signal into a delay equalizing network. Five steps of equalizer delay are available for selection by the module front-panel STEP switch. The selected delay provides one input from the equalizer delay network, and is supplied to emitter follower Q7. A second output is supplied from the end of the equalizer network to the difference amplifier stage that follows.

By varying the position of the STEP switch, the characteristics of the equalization curve are altered in such a way that the losses in the heads (due to aperture effect and head-to-tape transfer) are more closely compensated for without the introduction of phase errors. Final response adjustment for a selected setting is otained with the VERNIER EQUALIZATION control on the front panel.

Output FM from the difference amplifier (Q8 and Q9/Q10) is amplified through a feedback amplifier (Q11/Q12) and further amplified through the buffer series amplifier (Q13/Q14). Output for the Dropout Compensator module is amplified through a series amplifier (Q15/Q16). The outputs to either the FM Filter section or the FM Reference module are supplied through the contacts of relay K4. The relay condition determines which circuit receives the tape FM playback signal.

In the second function of the FM Equalizer section (to provide an indication for the CRO), the input signal is supplied from the input emitter follower Q20 to another emitter follower Q27. The signal is then applied to a detector Q28. This detected FM is coupled through a common base amplifier, controlled by the gate balancing potentiometer, and emitter follower Q30.

Pulses at a 960-Hz rate (4XTW) are supplied from the FM Switch module to the FM Equalizer module. The trailing edge of the 4XTW pulses trigger monostable multivibrator (MSMV) Q21/Q22 into its quasi-stable state, where it remains for 440 microseconds and then reverts back to its quiescent state. The transition from quasi to quiescent state results in a negative-going waveform that triggers the succeeding MSMV (Q23/Q24) into a similar sequence of events. Thus, the output of Q23/Q24 is a waveform that triggers chopper amplifier Q25 in such a way that the voltage at the collector of Q25 is driven to minus six volts for a short duration before and after the head-switching interval.

The voltage at the collector of Q25 during the chopped interval prevents the detected FM level from passing from transistor Q30 to emitter follower Q26. This condition provides a reference level for the CRO and results in a clean display of the relative output of each head, without the undesirable effects on the waveform that occur during the head overlap period. Detected FM is fed from the emitter of Q26 to MONITOR LEVEL potentiometer R176, and then to the CRO Switcher. Potentiometer R176 serves as a convenient level adjustment to accommodate a wide range of head output levels.

Equalizer Input and Amplifier

Input FM from the FM Switcher module is coupled through pin 17 of P1 on the FM Equalizer module, and to the base of Q20. This transistor is an emitter follower that buffers the module input from the lowpass filter input. The filter consists of capacitors C125, C124, and C123, and tunable inductors L73 and L72. The inductors are adjusted to provide a flat response of plus or minus 0.1 dB from 0.1 to 14 MHz, to the base of Q19. See figure 70.

Transistor Q19 is an emitter follower and buffer for the output of the filter. Transistors Q17 and Q18 form a series amplifier with a unity gain that serves as a delay-line driver.

Equalizer Delay and Difference Amplifier

The output from series amplifier Q17/Q18 is applied through resistor R90 to a delay line having two outputs. One is the receiving-end output which is unterminated and applied to the base of Q8. This is the upper-half of the difference amplifier and is composed of transistor Q8 and feedback amplifier Q9/Q10. See figure 71.

A second output from the delay line is taken from the "upstream" or sending-end of the delay line

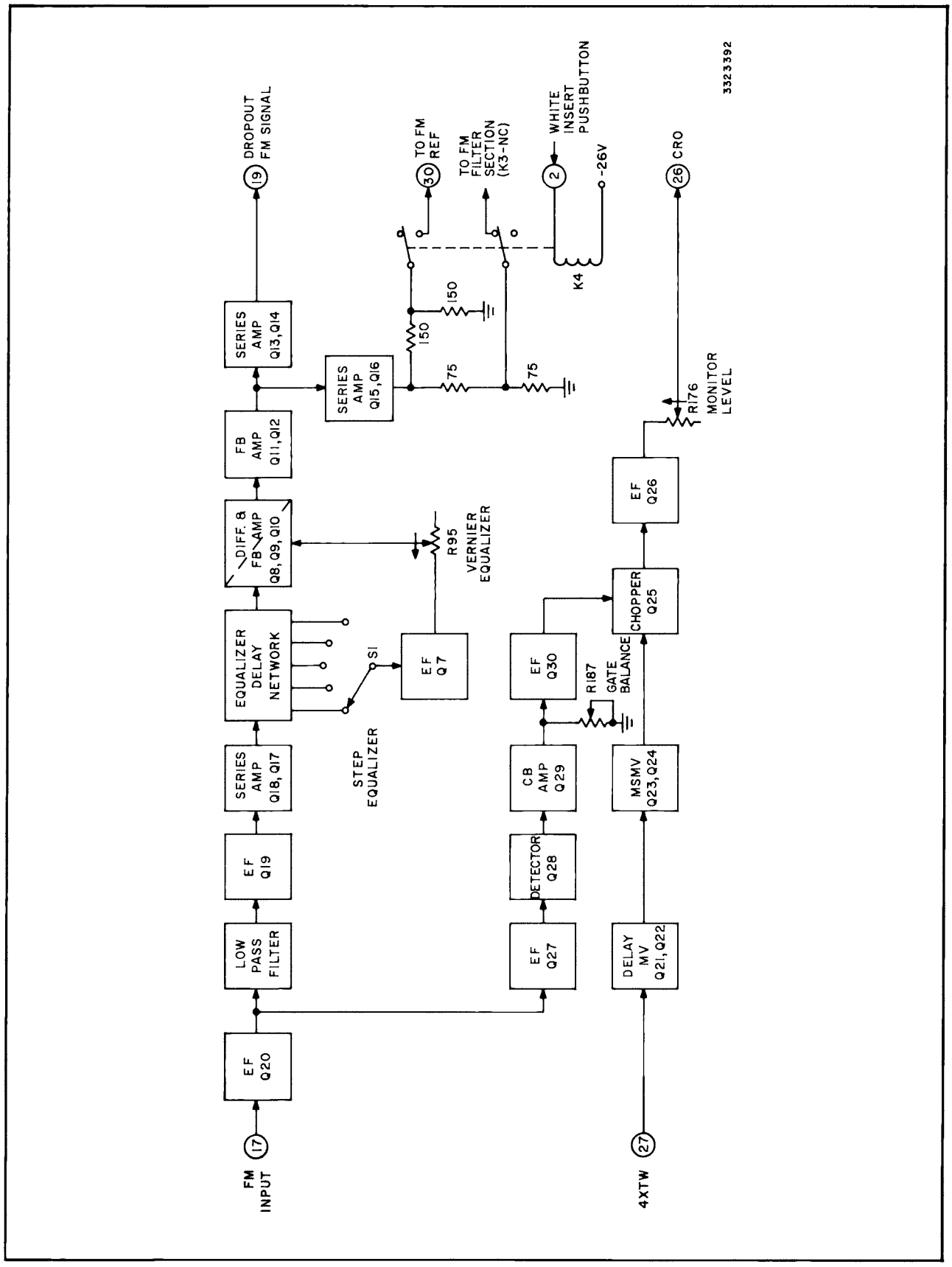
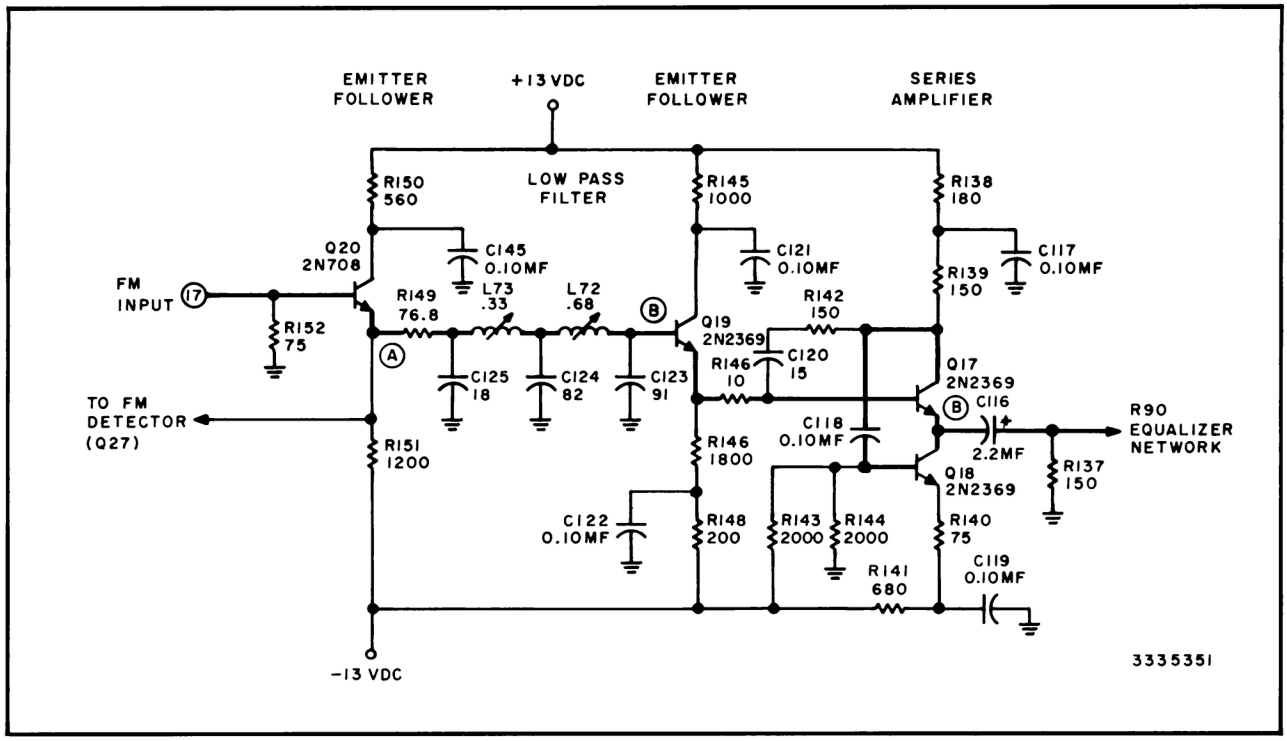
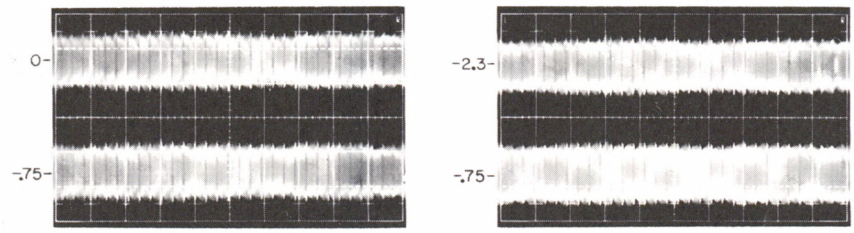


Figure 69—FM Equalizer Section of the FM Equalizer Module, Block Diagram





A. Top: P1 pin 17
Bottom: Q20 emitter
Both: .2 v/cm, .2 ms/cm

B. Top: Q19 base
Bottom: Q17 emitter
Both: .2 v/cm, .2 ms/cm

All waveforms in PLAY mode.

Figure 70—Equalizer Input and Amplifier, Schematic Diagram and Typical Waveforms

through step switch S1. This output is coupled to the base of isolation amplifier Q7 and is ac-coupled to the variable voltage divider network consisting of resistor R93 and VERNIER EQUALIZATION potentiometer R95. The output of the divider network is applied to the base of Q9, which with Q10 forms the feedback amplifier portion of the difference amplifier stage.

Operation of the delay line, equalization voltage divider, and difference amplifier provides the familiar "cosine equalization", which is similar to that circuit in the Playback Amplifier modules, and described there for those modules. Although this circuit is closely similar in operation, slight differences allow for additional "cosine equalization".

As in the Playback Amplifier module circuit, the delay line output is unterminated and results in a waveform at the base of Q8 that is flat in frequency. Five taps located further upstream on the delay line represent different delay-line lengths, with the length increasing from step 5 to step 1, respectively.

With the STEP switch in position 5, the delay line electrical length from this tap to the output is identical to the circuit in the Playback Amplifier modules. This results in the same "turnover frequency" (the frequency at which the equalized amplitude remains constant for all settings of VERNIER EQUALIZATION potentiometer R95) as in the Playback Amplifier modules. The signal appearing at the base of Q7 is varying in amplitude due to the reflections

from the unterminated output. This variation in amplitude follows the same cosine function as in the Playback Amplifier modules.

The front-panel VERNIER EQUALIZATION control (R95) varies the amplitude of the cosine function, which is then applied to the base of Q9. The resultant signal at the output of the difference amplifier has a characteristic that varies with frequency in accordance with the function 1 — A cos Θ, where R95 controls the amplitude of A. With potentiometer R95 set fully clockwise, the value of A is zero, and the output of the difference amplifier is flat with frequency. Intermediate positions of R95 cause the difference amplifier output to vary, with the shape of the curve determined by (1 — A cos Θ) function.

In HIGHBAND operation, the STEP switch is normally set to position 5, and proper equalization is then determined by the setting of the EQUALIZATION controls in this module and in the Playback Amplifier modules. The correct settings are those that yield a flat *multiburst* response on the CRO and minimum system difference gain. When choosing another standard (and/or with changing characteristics of the heads) it may be necessary to change the STEP switch position. The position selected should be one that, in conjunction with the VERNIER EQUALIZATION controls, yields a flat *multiburst* frequency

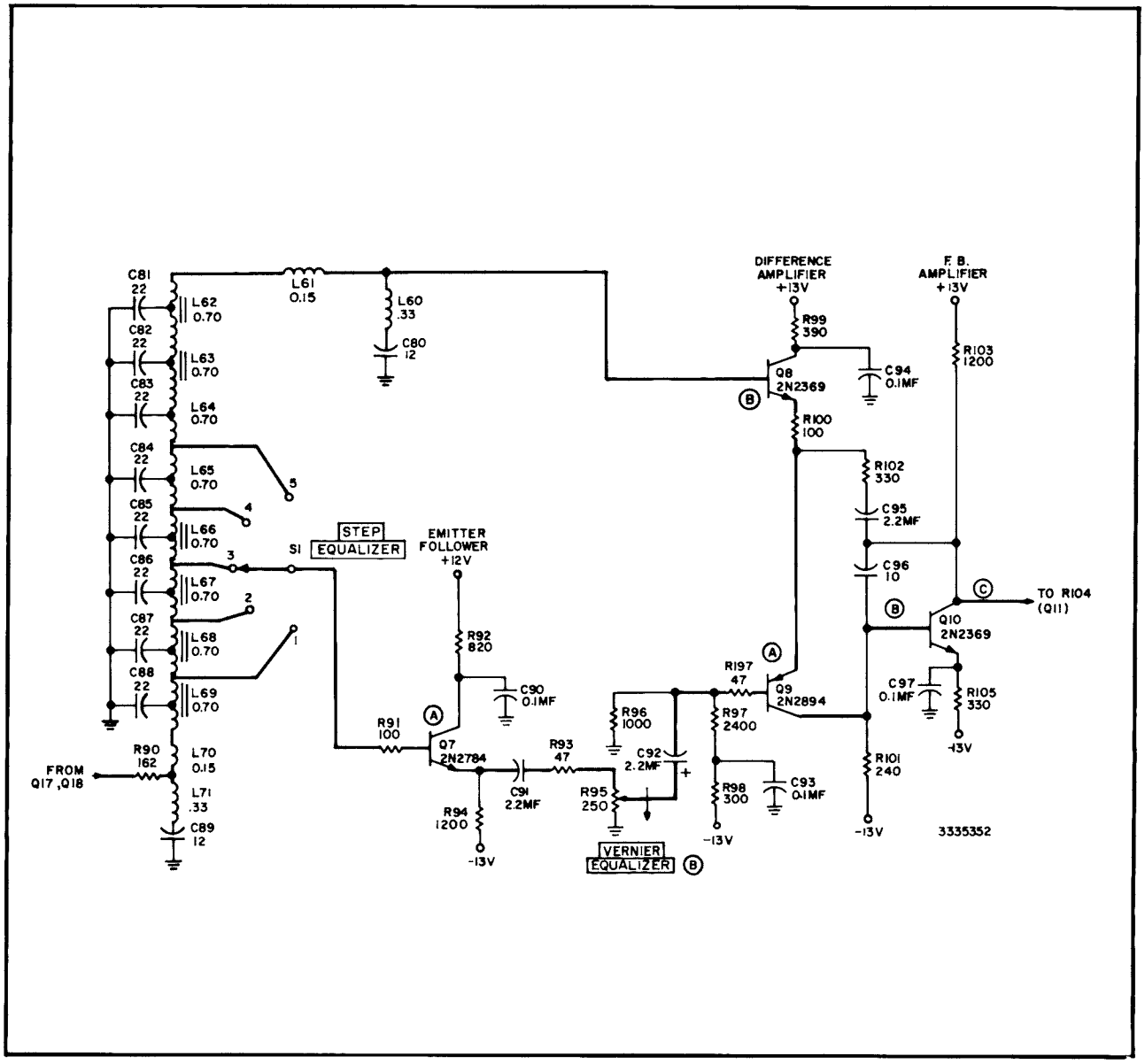
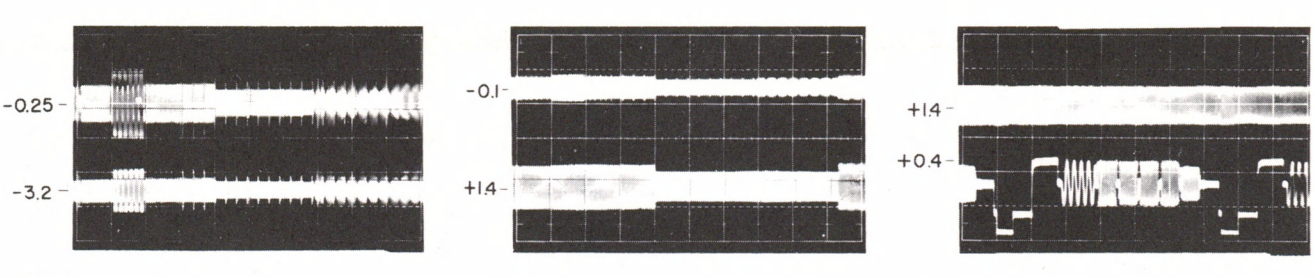


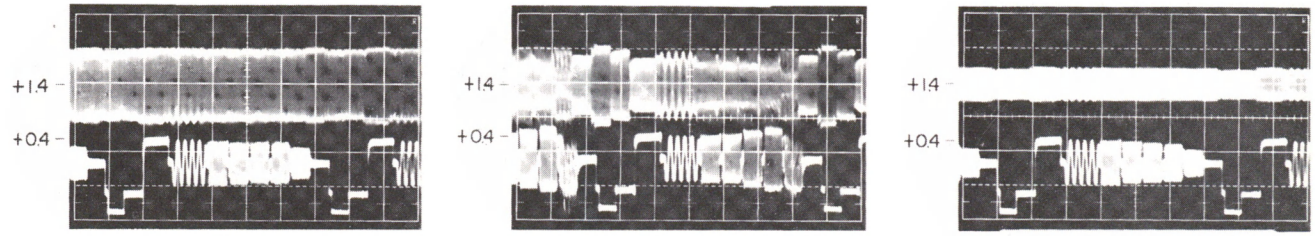
Figure 71—Equalizer Delay and Difference, Schematic Diagram and Typical Waveforms



A. Top: Q7 base
Bottom: Q9 base
Both: 0.1 v/cm, 0.2 ms/cm

B. Top: Q8 base
Bottom: Q10 collector
Both: 0.5 v/cm, 0.2 ms/cm

C. Top: Q10 collector
Bottom: DEMOD OUT TP1
Both: 0.5 v/cm, 10 μs/cm
Switch Position 5



C2. Top: Q10 collector
Bottom: DEMOD OUT TP1
Both: 0.5 v/cm, 10 μs/cm
Switch Position 1

C3. Top: Q10 collector
Bottom: DEMOD OUT TP1
Both: 0.5 v/cm, 10 μs/cm
Switch Position 5
R95 Maximum

C4. Top: Q10 collector
Bottom: DEMOD OUT TP1
Both: 0.5 v/cm, 10 μs/cm
Switch Position 5
R95 Minimum

All waveforms in PLAY mode.

Figure 71—Equalizer Delay and Difference, Schematic Diagram and Typical Waveforms (Continued)

response and minimum differential gain. The "turnover frequency" at each position of the STEP switch is as follows:

SWITCH POSITION	*TURNOVER FREQ (MHz)*
1	8.0
2	9.2
3	10.5
4	13.0
5	16.0

The equalization signal that appears at the output of the difference amplifier on the collector of Q10 actually is of the form:

$(1 - A \cos \Theta)\ (1 - B \cos \phi)$ where:

A = determined by EQUALIZATION controls on Playback Amplifier modules.

B = determined by VERNIER EQUALIZATION (R95) control on this module.

Θ = turnover frequency in the Playback Amplifier modules.

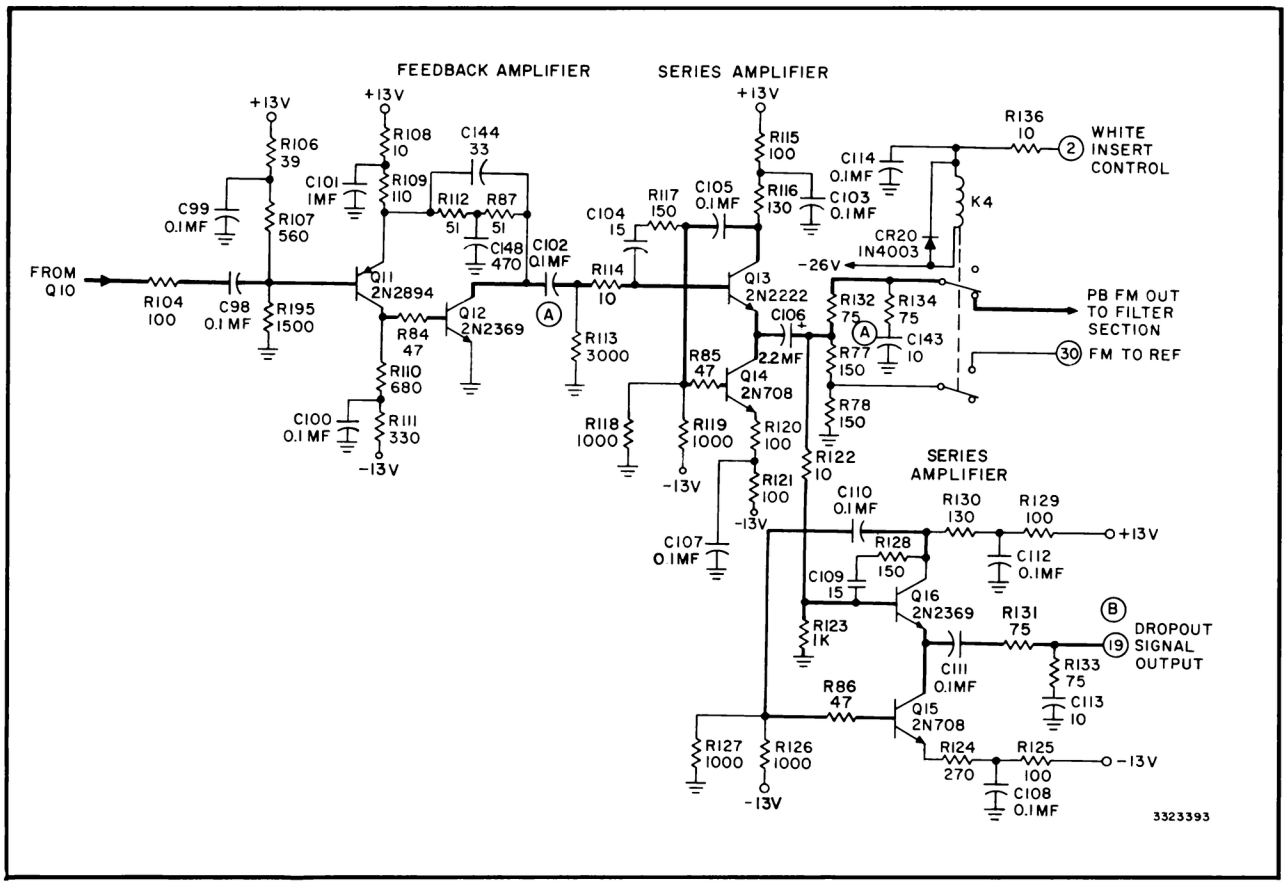
ϕ = turnover frequency in this module.

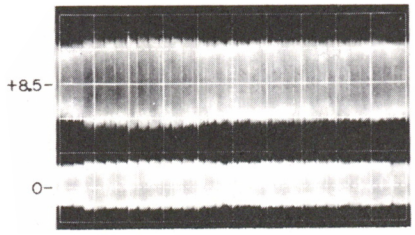
When the STEP switch is in position 5, the turnover frequencies are identical, and the expression takes on the form: $1 - (A + B) \cos \Theta + AB \cos^2 \Theta$. For different positions of the STEP switch, the expression becomes more complicated, but results in an equalization characteristic that complements the head output characteristic due to aperture losses. The output from the collector of Q10 is then applied via resistor R104 and capacitor C98 to the feedback amplifier that follows.

Amplifiers and Equalizer Output

Equalized FM is coupled through capacitor C98 to the base of Q11 in the feedback amplifier using transistors Q11 and Q12. The collector output of Q11 is coupled directly to the base of Q12. Feedback is from the collector of Q12 through the RC network using R87 and R112 and C144, to the emitter of Q11. The amplifier produces a gain of approximately two to the equalized FM signal. See figure 72.

Capacitor C102 couples the amplified FM signal from the feedback amplifier to series amplifier Q13/Q14. Coupling from the collector of Q13 to the base of Q14 is through capacitor C105. The combined outputs from the emitter of Q13 and collector of Q14





A. Top: Q12 collector
Bottom: Junction R106, R77
Both: .5 v/cm, .2 ms/cm
PLAY mode

Figure 72—Amplifiers and Equalizer Output, Schematic Diagram and Typical Waveforms

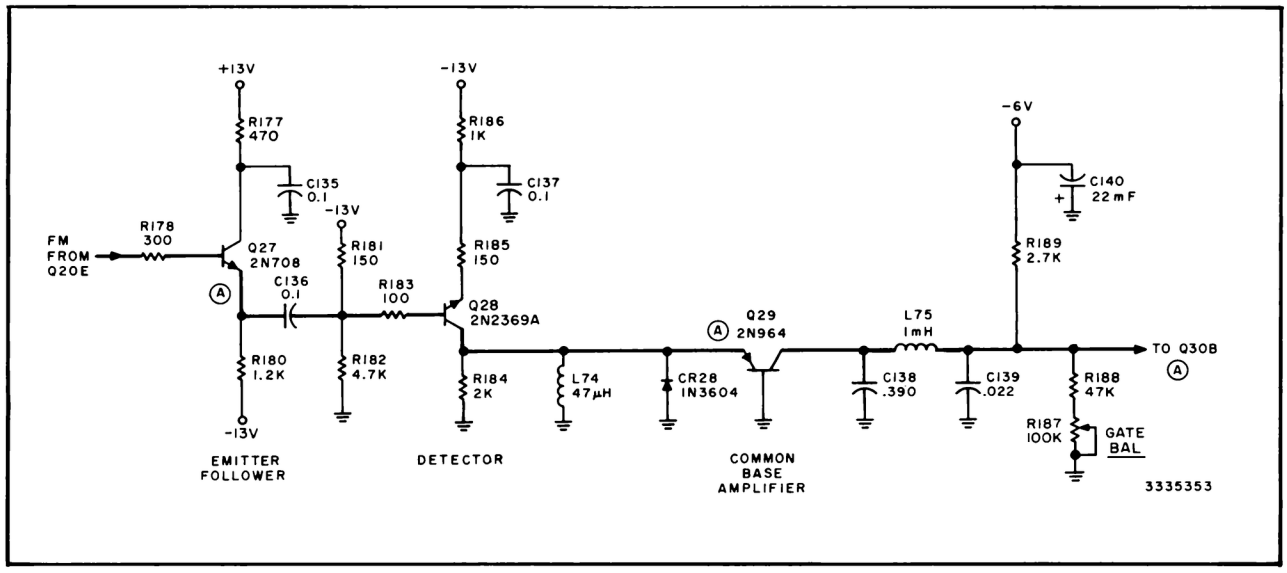
(both are in phase) is coupled through capacitor C106 to two paths.

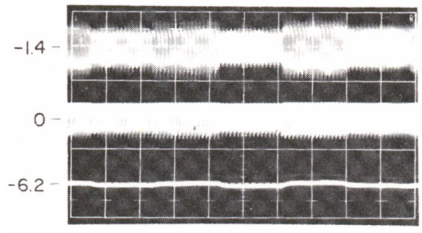
One output from series amplifier Q13/Q14 passes through the contacts of relay K4. When white insert is desired for tests, the relay closes and supplies the FM output via pin 30 of P1 to the FM Reference module. Under normal playback conditions, relay K4 remains deenergized and the normally-closed contacts of the relay connects playback FM to the FM Filter section of this module.

The second path from series amplifier Q13/Q14 is supplied to a series amplifier using transistors Q15/Q16. This amplifier functions identically to Q13/Q14. Its output is coupled through capacitor C111 and R131 to the Dropout AGC unit via pin 19. (This module is an accessory item.) Resistors R131 and R132 provide sending-end termination for the outputs from both series amplifiers.

FM Signal Detection

FM is coupled through resistor R178 to the base of Q27. This transistor isolates the FM signal and supplies it through capacitor C136 to the base of Q28. Transistor Q28 amplifies the signal prior to detection. See figure 73.





A. Top: Q27 emitter, 0.2 v/cm
Middle: Q29 emitter, 1 v/cm
Bottom: Q30 base, 5 v/cm
All: 0.5 ms/cm

PLAY mode

Figure 73—FM Detector, Schematic Diagram and Typical Waveforms

Amplified FM from the collector of Q28 is applied to diode detector CR28. The FM envelope is then detected through the diode. This detected signal is applied to the common base amplifier Q29.

Detected FM from diode CR28 passes through Q29 and to emitter follower Q30. GATE BALANCE potentiometer R187 adjusts the detected FM level at the base of Q30.

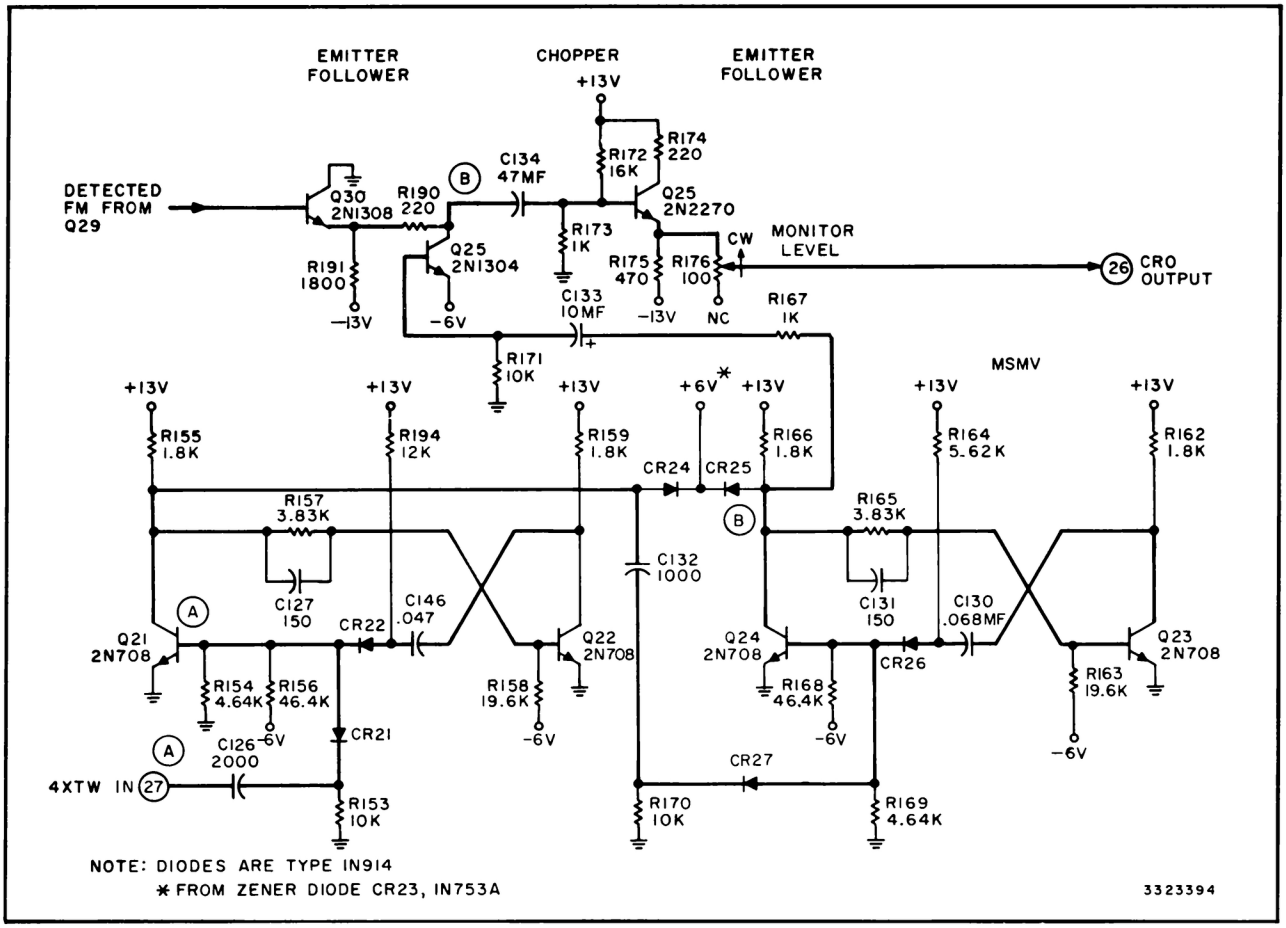
Multivibrators and Monitor Output

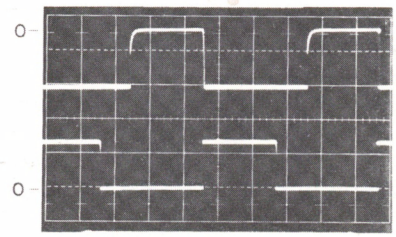
Detected fm is supplied to the base of emitter follower Q30 from the collector of Q29. The emitter output from Q30 is supplied through resistor R190 to the collector output of chopper transistor Q25. Refer to figure 74.

Detected fm, chopped at a 960-Hz rate, is coupled from the collector of Q25 through capacitor C134 to the base of emitter follower Q26. This transistor couples the detected and chopped fm from the module via pin 26 to the CRO Switcher for presentation on the CRO. Potentiometer R176 permits adjustment of the detected signal level on the CRO.

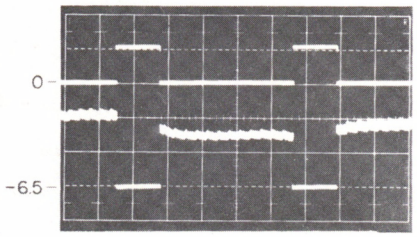
Switching pulses at 960-Hz, or four times the tonewheel rate (4XTW) are supplied from the FM Switcher module via pin 27 of P1. These pulses are coupled through capacitor C126 and diode CR21 to trigger the delay multivibrator using transistors Q21 and Q22. This is a standard monostable multivibrator.

Negative portions of the 4XTW signal pass through diode CR21 and are applied to the base of Q21. During quiescent condition of the delay multivibrator, transistor Q22 is cut off and Q21 is conducting. With reception of a negative pulse through diode CR21, the multivibrator changes state and remains in that condition for approximately 440 microseconds, as determined by RC network R194 and C146, the plus 13-volt supply, and the collector potential of Q22.





A. Top: P1 pin 27
Bottom: Q21 collector
Both: 5 v/cm, 0.2 ms/cm



B. Top: Q24 collector, 5 v/cm
Bottom: Q25 collector, 0.5 v/cm
Both: 0.2 ms/cm

Waveforms in PLAY mode.

Figure 74—Multivibrators and Test Output, Schematic Diagram and Typical Waveforms

After an elapse of 440 microseconds, the negative-going trailing edge of the pulse from the collector of Q21 forward biases diode CR27 and cuts off transistor Q24 which was normally on. The resulting postive pulse from the collector of Q24 is ac-coupled to the base of chopper transistor Q25 to cause it to conduct. The time duration of this positive pulse is approximately 370 microseconds as determined by RC network R164 and C130, and the reduced potential caused by resistor R162 on the collector of Q23.

With transistor Q25 conducting for 370 microseconds starting at 185 microseconds before the 4XTW pulse, it causes the detected fm playback signal to be chopped for 185 microseconds before and 185 microseconds after the 4XTW pulse. During normal playback, the detected fm level displayed on the CRO is chopped for a period which straddles the head-switching interval.

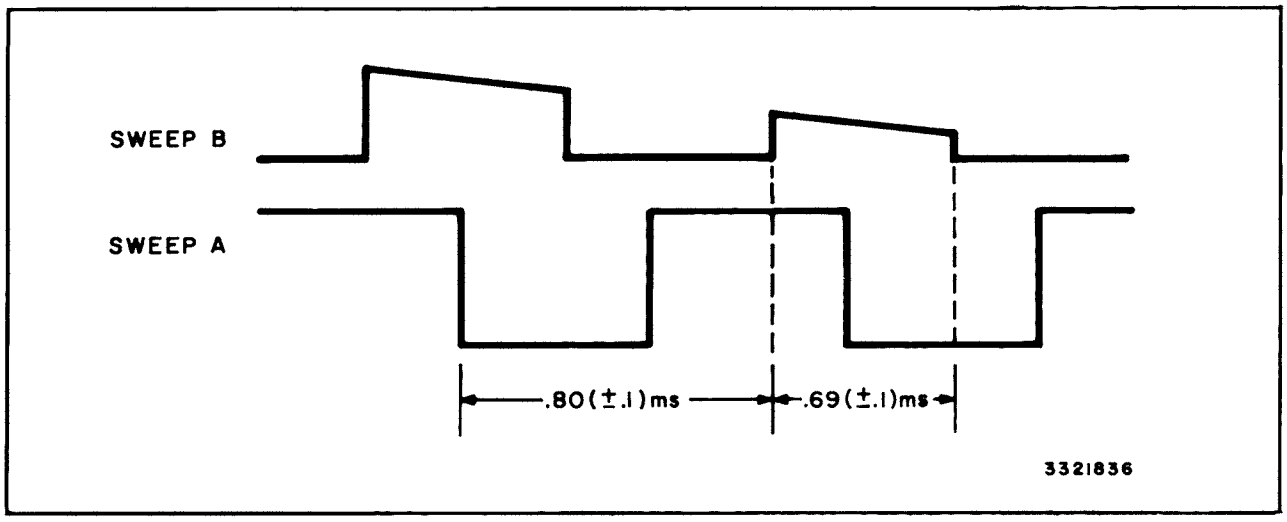


Figure 75—Detected FM and Chopper Timing Diagram

CIRCUIT DESCRIPTION—FM FILTER SECTION

General

Tape FM from the FM Equalizer section of this module is fed through the normally-closed contacts of relay K3 to filter driver Q5/Q6. Energizing the coil of relay K3 selects FM with white reference through the relay contacts. The latter condition exists when the machine is in E-E, SETUP, RECORD, and PLAY mode when the WHITE INSERT pushbutton switch is depressed. See figure 76.

The selected signal is supplied to the filter driver stage (Q5, Q6) which has a gain of unity and serves as a buffer between the filters and external circuits. Output from the amplifier is supplied to either the highband or lowband filters, depending on the standard selected with the Standards Generator and the condition of the E-E bus. The highband filter is always selected when the machine is in E-E mode. For playback, filter selection is determined by the standard in use. Filter selection is further described below.

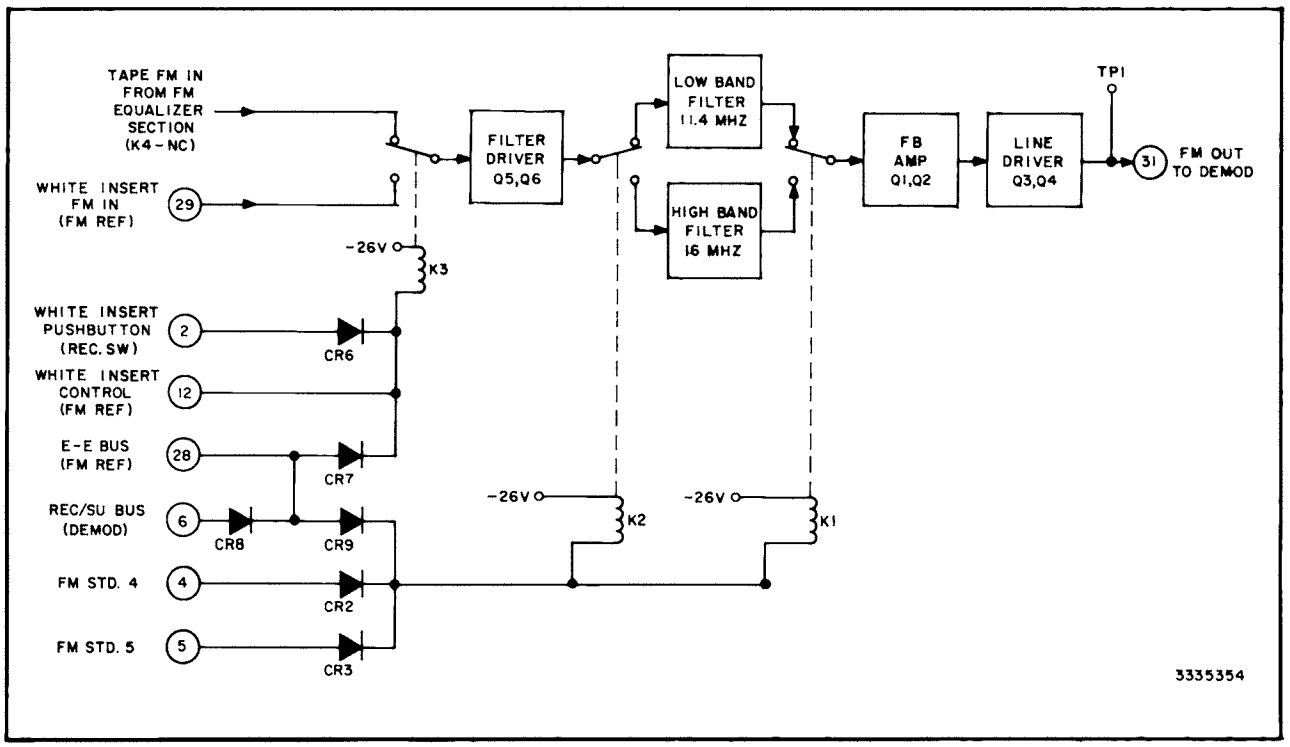


Figure 76—FM Filter Section, Block Diagram

Both the highband and lowband filters are of similar construction. Each has an amplitude equalizer and lowpass filter in addition to its basic rolloff filter network. A phase equalizer is also included for the lowband filter.

Filtered FM is supplied to feedback amplifier Q1/Q2 which compensates for losses realized through filtering. Amplified FM is then fed through a line driver which provides buffering between the filter and external circuits. FM leaves the module via pin 31 and is supplied to the Demodulator module.

Input Control and Filter Driver

Input selection is accomplished by means of two control busses or with the WHITE INSERT push-button, in conjunction with relay K3. See figure 77. When E-E operation has been selected with the E-E switch (S1 on the Modulator AFC module) and the machine is operating in STANDBY, WIND or STOP modes, the coil of relay K3 is energized through pin 28 of P1 and forward-biased diode CR7, and the grounded E-E bus. Similarly, in RECORD or SETUP modes, relay K3 is energized through pin 6 and forward-biased diode CR8, and the grounded record/setup bus. Thus, in all these modes, relay K3 is energized to select FM from the FM Reference module through pin 29 of P1. In the above events, FM is supplied from the Modulator module and passes through the FM Filter section in the E-E monitoring system.

If the machine is playing back a recorded tape, neither the E-E bus nor the record/setup bus is at ground level, therefore relay K3 remains deenergized. FM is now fed directly from the FM Equalizer section through the normally-closed contacts of relay K3 to the filter circuits.

Depressing the WHITE INSERT pushbutton (S1 on the Record Switch module) while the machine is operating in PLAY mode causes the three following operations to occur:

1. A transfer relay in the FM Equalizer module becomes energized by a grounded control bus through switch S1 and pin 2. This causes equalized tape FM to be fed to the FM Reference module.

2. A relay at the input of the FM Reference module switches from Modulator module E-E FM to tape FM from the FM Equalizer module. This relay is controlled by a bus which is grounded through switch S1, and passes the grounded level through diode CR6 and pin 2 of P1. White reference is thus inserted into tape FM by the FM Reference module, and the composite signal appears at pin 29 as the FM-plus-reference signal.

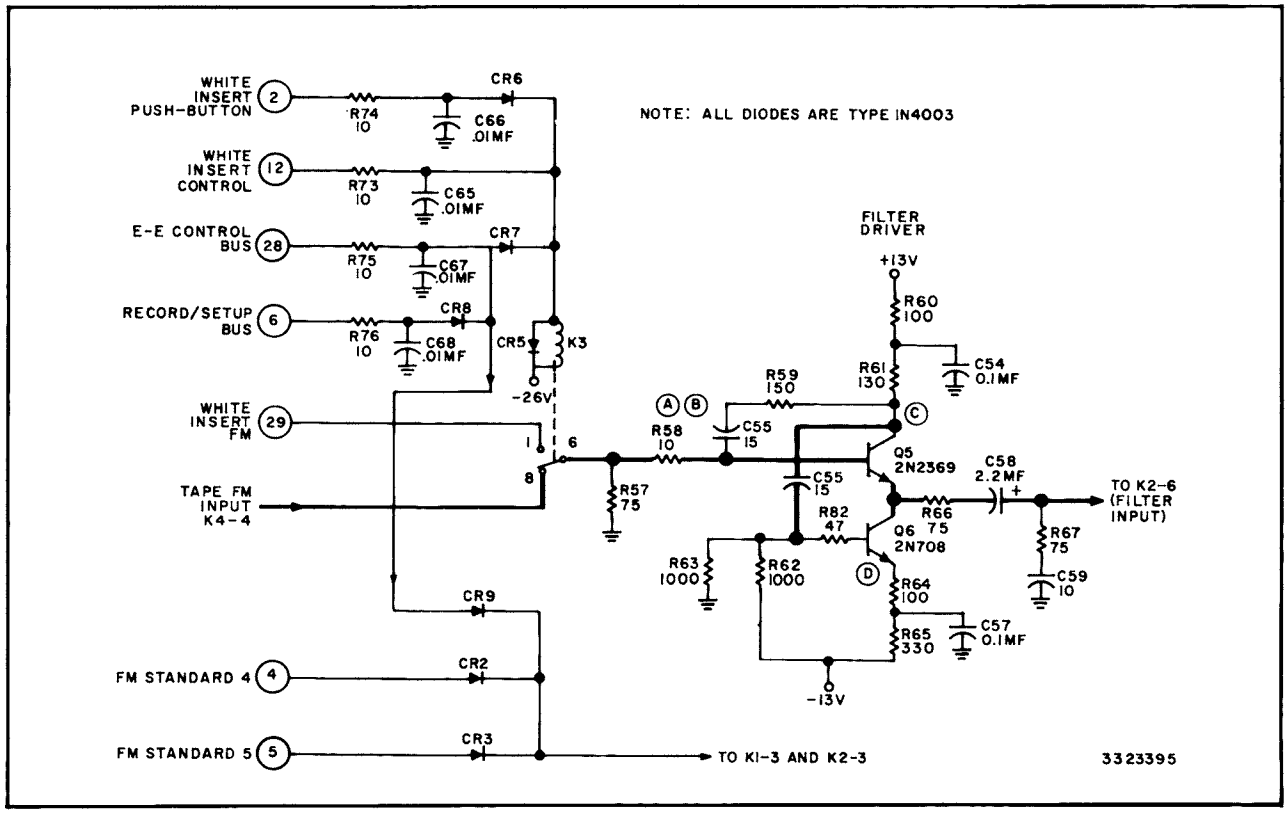
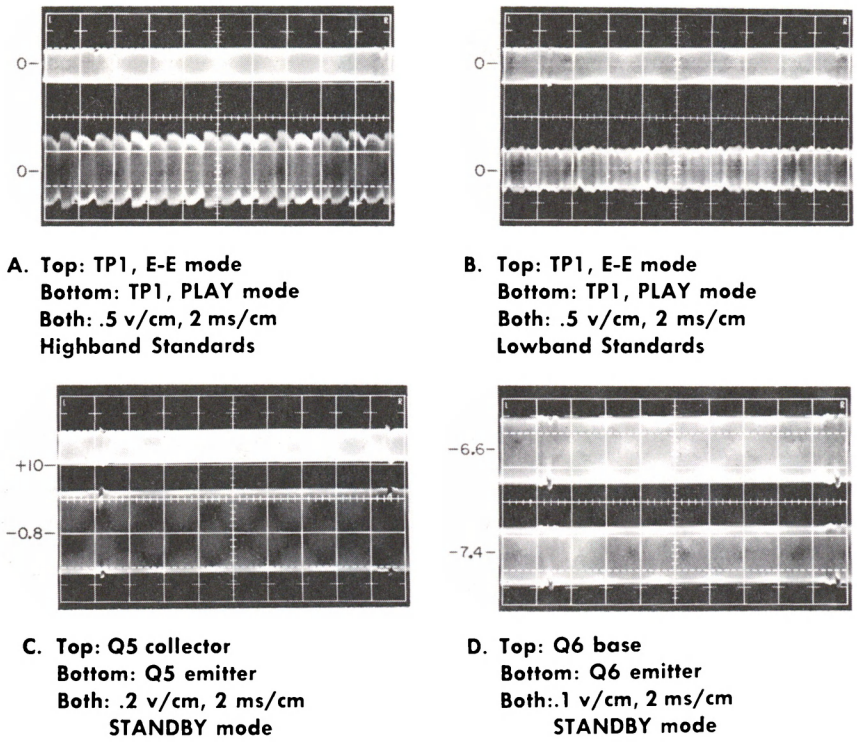


Figure 77—Input Control and Filter Driver, Schematic Diagram and Typical Waveforms



A. Top: TP1, E-E mode
Bottom: TP1, PLAY mode
Both: .5 v/cm, 2 ms/cm
Highband Standards

B. Top: TP1, E-E mode
Bottom: TP1, PLAY mode
Both: .5 v/cm, 2 ms/cm
Lowband Standards

C. Top: Q5 collector
Bottom: Q5 emitter
Both: .2 v/cm, 2 ms/cm
STANDBY mode

D. Top: Q6 base
Bottom: Q6 emitter
Both:.1 v/cm, 2 ms/cm
STANDBY mode

Figure 77—Input Control and Filter Driver, Schematic Diagram and Typical Waveforms (Continued)

3. Relay K3 becomes energized by grounding its coil through switch S1 and diode CR6. Tape FM with inserted reference then passes through pin 29 of P1 and the contacts of relay K3 to the filter driver stage.

In summarizing, all modes except PLAY feed the FM signal to the filter driver stage with reference. In PLAY mode, input to the filter driver remains only as tape FM unless the WHITE INSERT button is depressed. In this case, the input is tape FM with white reference inserted.

The selected input signal from pin 6 of relay K3 is terminated by resistor R57 and fed through parasitic-suppressor resistor R58 to the base of Q5. Transistors Q5 and Q6 form a series amplifier with a gain of unity. The collector output from Q5 is ac-coupled through capacitor C56 to the base of Q6. Output from the series amplifier (or filter driver) is taken from the combined emitter of Q5 and collector of Q6 because both are in phase and provide a very low output impedance. This output is fed through sending-end terminating resistor R66 to match the filter input impedance, and coupled through capacitor C58 to the selected filter via relay K2.

Filter Selection

The highband and lowband filters are selected by relays K1 and K2 on the inputs and outputs of the filters. Selecting the E-E mode of operation while presently operating in STANDBY, WIND or STOP modes, energizes the relays by allowing a ground level to be supplied through pin 28 of P1. This level forward biases diode CR9 to allow current to flow through the relay coils. Energizing relays K1 and K2 selects the highband filter (16 MHz).

When the E-E bus is not grounded through WHITE INSERT switch S1 (as during PLAY mode), the proper filter is selected in accordance with the standard selected from the Standards Switcher panel. If one of the highband standards (525 HB or 625 HB) is selected, relays K1 and K2 are energized through either pin 4 or pin 5 and the associated forward-biased diode, and results in the selection of the highband linear rolloff filter. If a lowband standard (525 LB, 625 LB or 525 color) has been selected, the relays remain deenergized and the lowband (11.4 MHz) filter becomes activated. Table 7 lists the various conditions for filter band selections.

11.4-MHz and 16-MHz Linear Rolloff Filters

The lowband filter (11.4 MHz) and highband filter (16.0 MHz) are similarly constructed, therefore

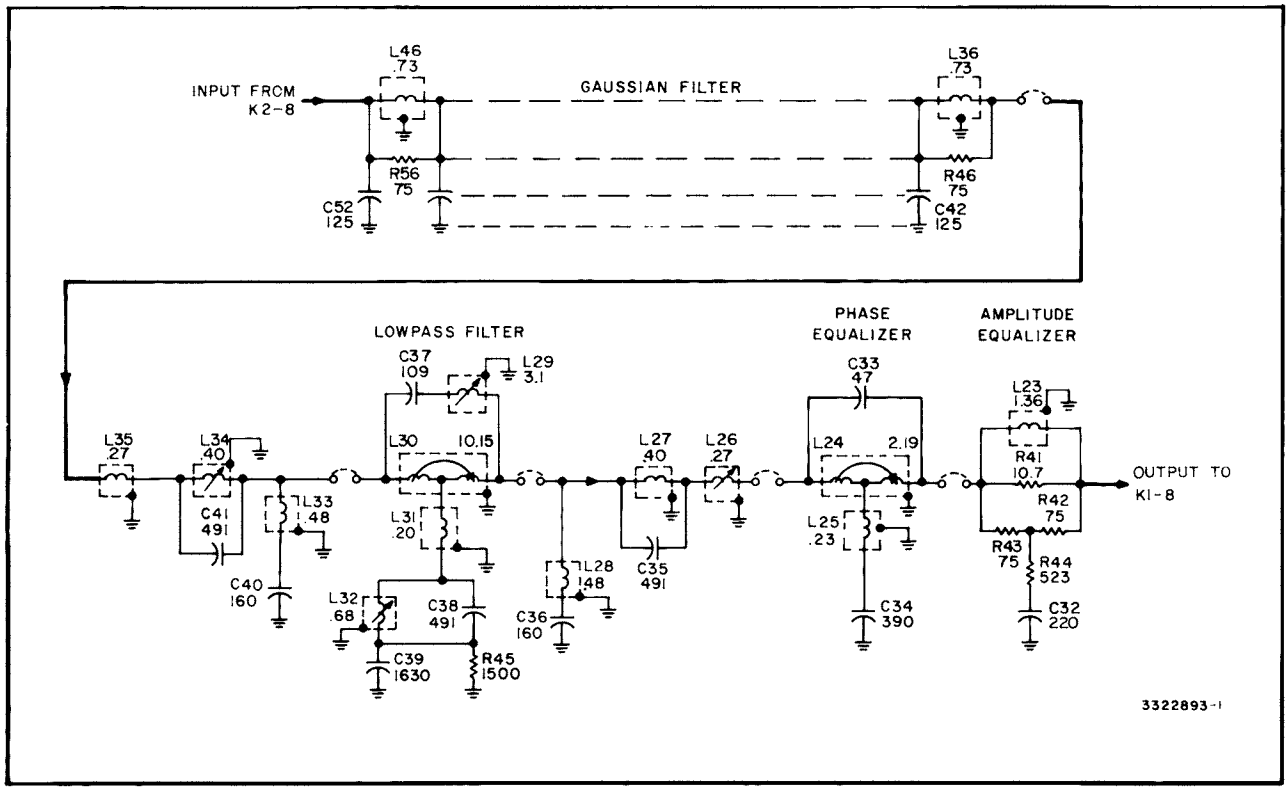


Figure 78—11.4-MHz Linear Rolloff Filter, Schematic Diagram

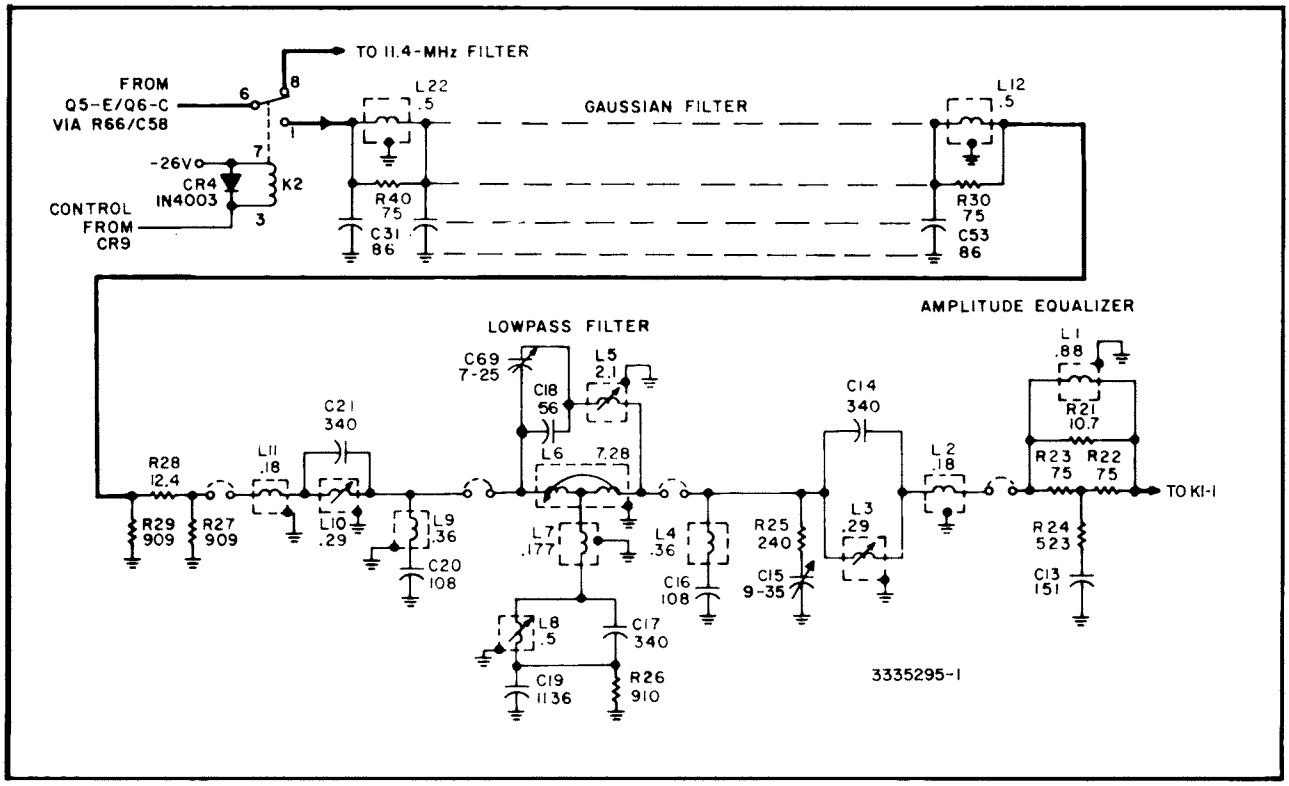


Figure 79—16-MHz Linear Rolloff Filter, Schematic Diagram

TABLE 7—FILTER BAND SELECTIONS

OPERATING MODE	*FUNCTION*	*STANDARD*				
		1 405/525 LB Mono	*2 625 LB Mono*	*3 525 LB Color*	*4 405/525 Highband*	*5 625 Highband*
PLAY	K1, K2	Off	Off	Off	On	On
	Filter (MHz)	11.4	11.4	11.4	16.0	16.0
E-E and RECORD	K1, K2	On	On	On	On	On
	Filter (MHz)	16.0	16.0	16.0	16.0	16.0

only the lowband filter is described. See figures 78 and 79. Each filter consists of basic networks that perform a specific function to produce a linear rolloff amplitude characteristic as a result of their combined response curves. These networks are: (1) gaussian network, (2) lowpass filter, (3) phase equalizer (in the lowpass filter only), and (4) amplitude equalizer.

In the gaussian network, a linear rolloff voltage-versus-frequency characteristic is obtained at the center section of the slope (figure 80-A). This is accomplished by a series of fixed inductors, capacitors and resistors which have a cumulative effect on the signal that produces the linear section. In the lowband filter, this network consists of inductors L36 through L46, capacitors C42 through C52, and resistors R46 through R56.

Filtering in the lowpass filter network produces a sharp null at the cutoff frequency of the filter (figure 80-B). Thus, in the lowpass filter, the point of minimum response is at exactly 11.4 MHz, which is the cutoff point of the linear rolloff slope. The lowpass filter network consists of inductors L26 through L35, capacitors C35 through C41, and resistor R45.

The phase equalizer network functions to produce a linear phase characteristic over the entire filter bandpass. The phase equalizer consists of transformer-inductor L24 with fixed inductor L25, and capacitors C33 and C34. It has negligible effect on the amplitude response.

The amplitude equalizer network consists of inductor L23, resistors R41 through R44, and capacitor C32. The purpose of this network is to extend the linearity at the low frequency end of the slope (figure 80-C).

Amplifier and Line Driver

Filtered FM is amplified through two stages to compensate for termination losses and filter attenuation. Amplified FM is then supplied through a line driver output stage that drives the transmission line between the FM Equalizer module and the Demodulator module. See figure 81.

Output from the selected filter is supplied through the contacts of relay K1 and capacitor C1 to the base of Q1. Resistor R1 terminates the filter output at 75 ohms. Amplified FM is taken from the collector of Q1 and coupled through R80 to the base of Q2, with feedback from Q2-collector to Q1-emitter. Both transistors provide an overall gain of 11 to the signal level and couple their output through capacitor C6 to the line driver stage. Capacitor C4 improves the high-frequency response.

Transistors Q3 and Q4 form a series amplifier with the collector output from Q3 ac-coupled through capacitor C9 to the base of Q4. The emitter output of Q3 is combined with the collector output of Q4 to provide for unity voltage gain and low output impedance. The common output is coupled through capacitor C11 and pin 31 of P1 to the Demodulator module. Resistor R19 terminates the output at 75 ohms. Resistor R20 and capacitor C12 terminate the line at high frequencies when the output impedance of the series amplifier becomes too high.

ADJUSTMENTS

FM Filter Section

The FM Filter Section has been carefully adjusted at the factory and settings should not be disturbed. All internal adjustments are of a factory-type that require special test equipment. The adjustments have been locked in place with a red or blue sealing compound to prevent accidental changes in settings. If service is required, contact your RCA field representative.

FM Equalizer Section

The FM Equalizer module has been carefully adjusted at the factory and should not be disturbed

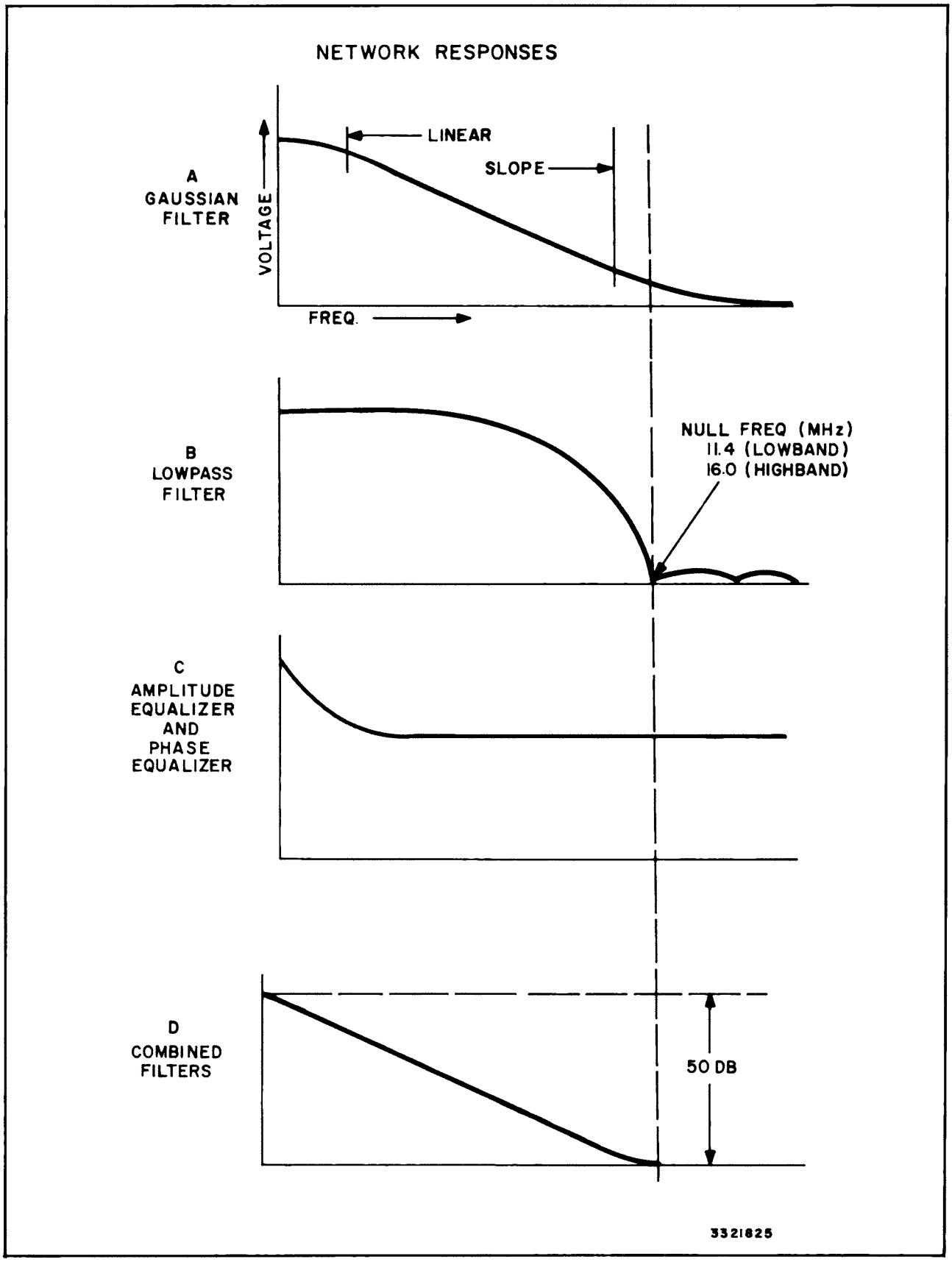
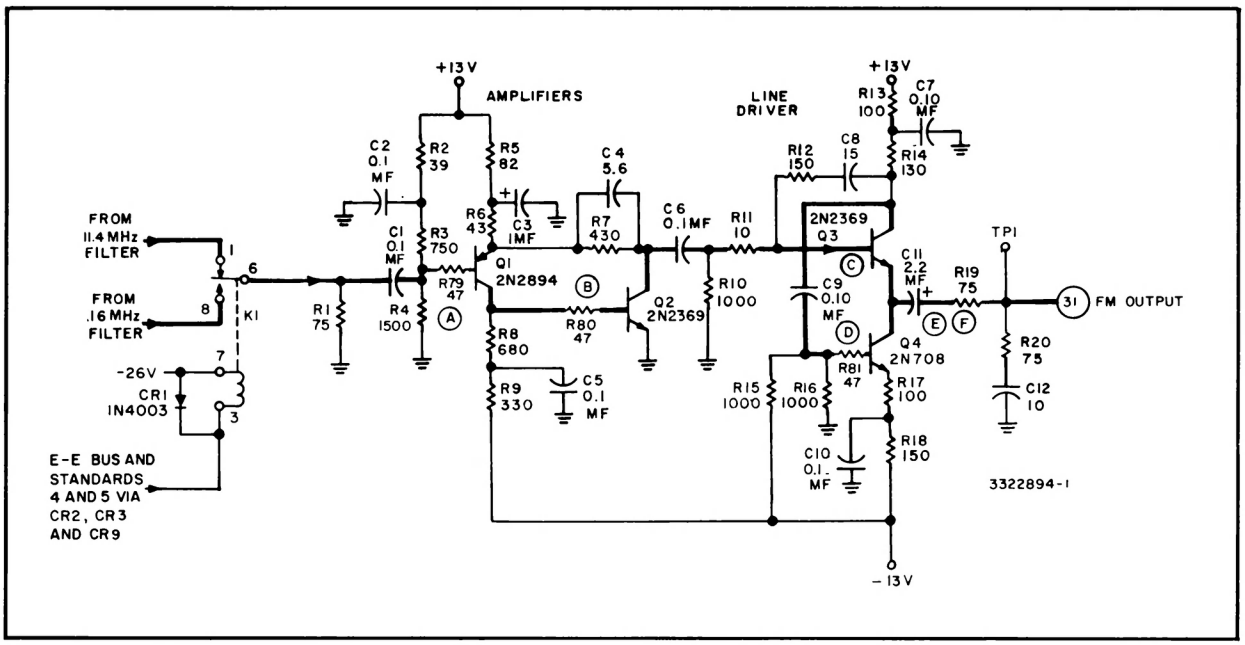


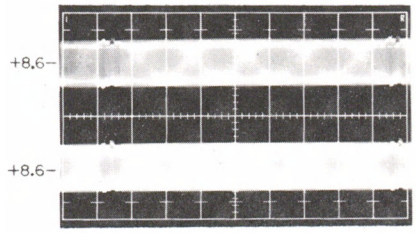
Figure 80—Filter Network Response Characteristics

unless positive determination is made that any other defect has been corrected and an adjustment is the only remaining requirement for optimum performance.

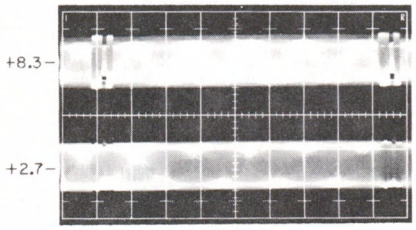
Although the adjustments described for this module are separated, they are directly related to each other and necessitate that both be performed if either is required. The should be performed in the order presented.

NOTE: Adjustments for inductors L21 and L22 are not described because special test equipment is required that is capable of measuring response definition of plus or minus 0.1 dB from 0.1 to 14.0 MHz. Consequently, the settings for these inductors are locked in place with red or blue sealant. Contact your RCA Service Company field office if service is required.

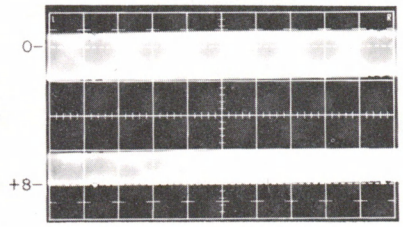




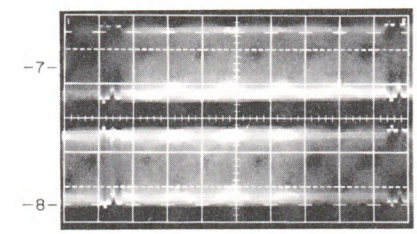
A. Top: Q1 base
Bottom: Q1 emitter
Both: .1 v/cm, 2 ms/cm



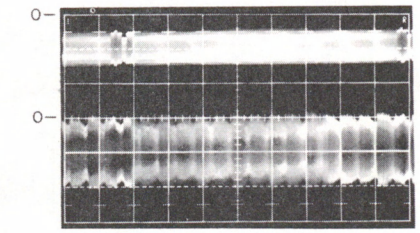
B. Top: Q2 base, .05 v/cm
Bottom: Q2 collector, 1 v/cm
Both: 2 ms/cm



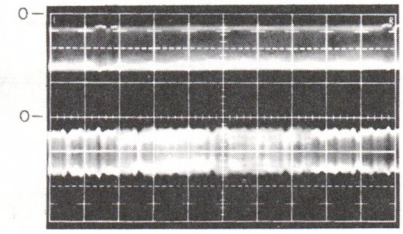
C. Top: Q3 base, 1 v/cm
Bottom: Q3 collector, .5 v/cm
Both: 2 ms/cm



D. Top: Q4 base
Bottom: Q4 emitter
Both: .2 v/cm, 2 ms/cm



E. Top: Q4 collector, E-E mode
Bottom: Q4 collector, PLAY mode
Both: 1 v/cm, 2 ms/cm
Highband Standards



F. Top: Q4 collector, E-E mode
Bottom: Q4 collector, PLAY mode
Both: 1 v/cm, 2 ms/cm
Lowband Standards

All waveforms in PLAY mode unless noted otherwise.

Figure 81—Output Amplifier and Line Driver, Schematic Diagram and Typical Waveforms

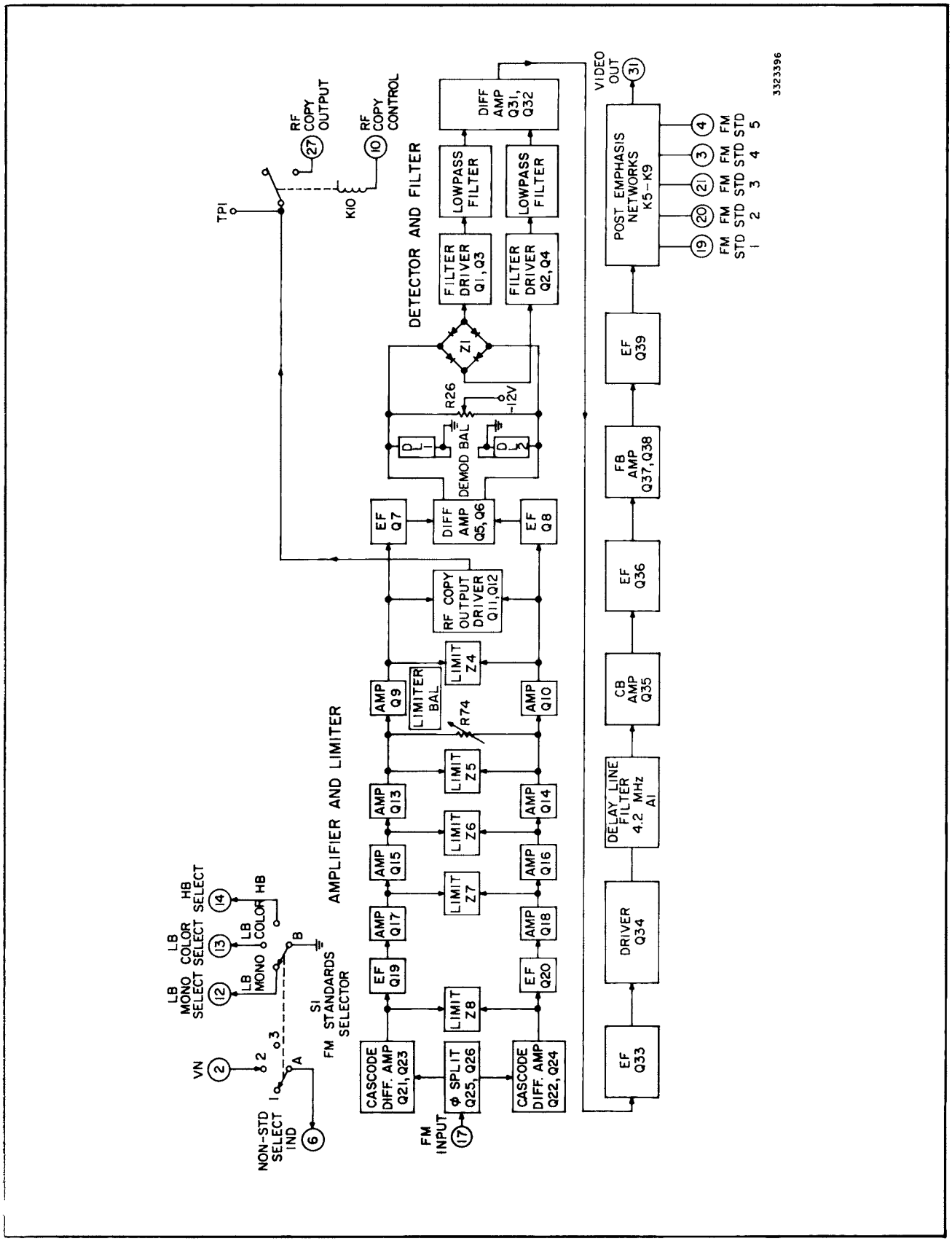


Figure 82—Demodulator Module, Block Diagram

Gate Balance Adjustment

Proceed as follows to adjust the gate balance potentiometer R187 and to check the chopper timing relationship with the chopped, detected fm signal:

1. Remove the FM Equalizer module and reconnect it to its slot through the module extender.

2. Press SW OUT button on the CRO switcher and observe the display in E-E (or connect oscilloscope to P1-26).

3. Adjust R187 for minimum residual signal on the display.

Monitor Level Adjustment

The CRO output level from the FM Equalizer module is adjusted with monitor level potentiometer R176. This adjustment should be performed only after the gate balance adjustment (described above) is complete. Proceed as follows:

1. Record a section of multiburst and a section of gray level carrier (noise test), in HB Standards.

2. Play back the recording and adjust equalizers for flat response while observing the multiburst signal.

3. Set the Playback Amplifier gain controls for 0.3 volt peak-to-peak measured at P1-31, while playing back the carrier recording.

4. Set R176 for 30 IRE units peak-to-peak under the above condition.

DEMODULATOR MODULE

CIRCUIT DESCRIPTION

General

The Demodulator module serves to amplify and limit playback FM supplied from the input source. The FM is equalized and filtered through the FM Equalizer module prior to demodulation. The Demodulator module supplies a replica output of the original video by passing the demodulated video through a post emphasis network.

FM supplied to the Demodulator is fed to phase splitter Q25/Q26 where outputs of opposite phase are supplied to dual-channel cascode differential amplifiers Q21/Q23 and Q22/Q24. Refer to block diagram, figure 82.

The cascode differential amplifier supplies its outputs to the first of five limiter stages. Each stage operates in push-pull with an associated differential amplifier and emitter follower for each channel. The opposite phases of the FM signal are balanced, amplified and symmetrically clipped prior to combining the phases for demodulation.

Output from the fifth limiter stage (Q9, Q10) is supplied to differential amplifier Q11/Q12. This differential amplifier then feeds an output from the module via relay K10 when the rf copy mode of operation is selected. This output, which is still in FM form, is supplied from the machine as the rf copy signal and is sometimes used directly for rerecording when a copy tape is to be made.

The fifth limiter stage couples its output with emitter followers Q7 and Q8 to the delay line drivers using differential amplifiers Q5 and Q6. Reflections from delay lines DL1 and DL2 produce narrow pulses as a result of the square-wave current pulses that enter the delay line. Each half of the push-pull circuit generates a positive or negative pulse at each corresponding input square-wave transition. Pulse repetition rate is therefore twice the instantaneous FM carrier frequency. See figure 87.

The quad diodes in Z1 are connected as a bridge rectifier that gates the push-pull positive and negative pulses from the delay lines to the proper push-pull input of filter drivers Q1 through Q4. The bridge supplies only negative pulses to transistor Q3, and only positive pulses to transistor Q4.

Subsequent integration (through filtering) of the constant-width pulses from the bridge rectifier develops an average voltage with an amplitude that is dependent on only the pulse repetition rate. Thus, in the push-pull phase with positive pulses, the higher the pulse repetition rate becomes, the more positive will be the output voltage. A similar situation exists in the negative phase of the push-pull circuit, where a negative average voltage is developed.

The Modulator module has originally produced a carrier frequency that was proportional to the instantaneous level; therefore, the demodulation process utilizes the inverse of this relation to develop an output voltage that is proportional to the carrier frequency and thereby reproduce the original video.

The balanced output from the bridge is prefiltered to remove some of the higher frequency FM

components and fed to differential amplifier Q31, Q32, which converts the signal to single ended. Driver stages Q33, Q34 amplify the single ended signal and supply it to a Golay filter, 4.2 MHz for domestic standards or 5 MHz for international standards.

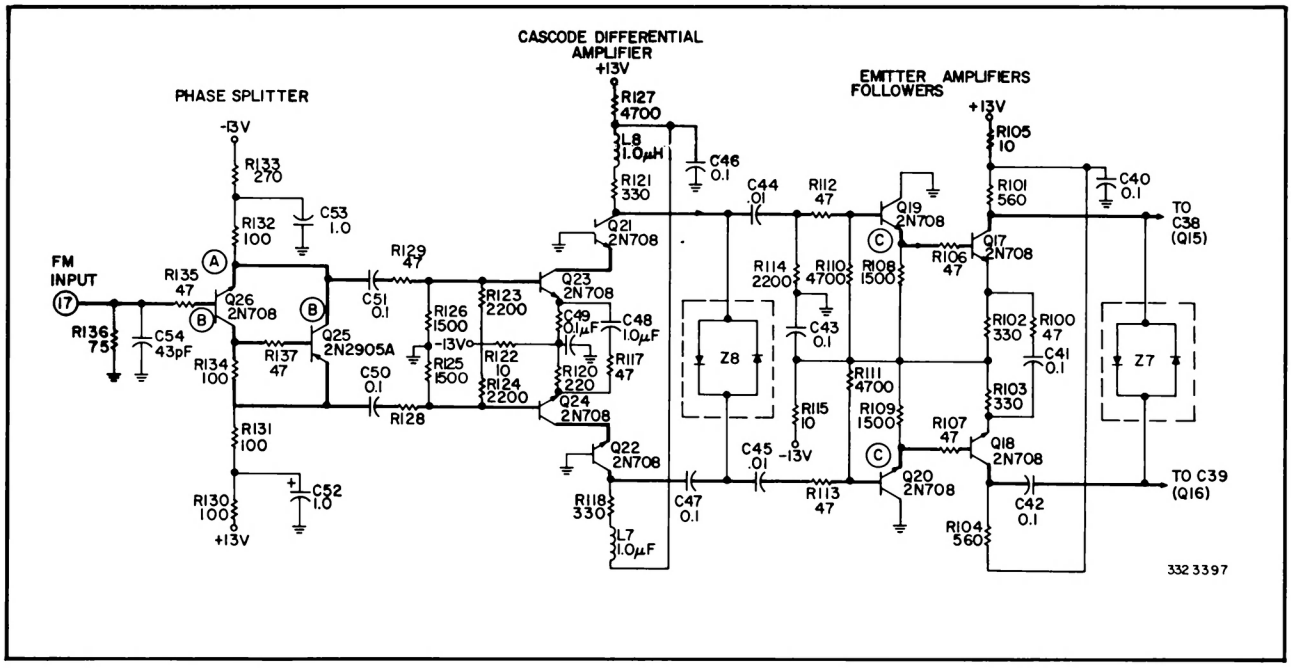
Filtering removes unwanted residual high frequency components, supplying a signal at the output that is a varying dc average of the pulse input. Since the dc variations in the filtered signal are proportional to the frequency of the input pulses, the output signal is a replica of the original video modulating signal.

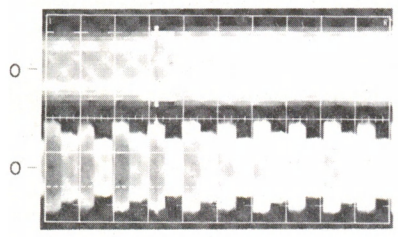
The output of the filter is fed to a series of video amplifiers and buffer stages to the post emphasis network. The correct network for the selected standard is controlled by signals from the Standards Generator module. The FM standard signal selects the proper relay, K5 through K9, to provide the proper amount of post-emphasis to the video signal which compensates for the same amount of pre-emphasis added during the recording process.

Input and Phase Splitter

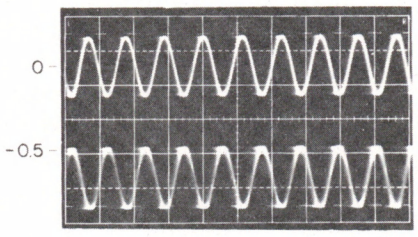
An input signal having a level of 0.5 volt peak-to-peak (nominal) is fed through parasitic suppression resistor R135 to the base of Q26. The input transmission line is terminated by resistor R136. See figure 83.

Transistors Q25 and Q26 operate as a complementary push-pull emitter follower. In effect, Q26 is an emitter follower driving one output with an in-phase signal, while Q25 is another emitter follower driving the second output with an out-of-phase signal developed across R134, the collector-load resistor for

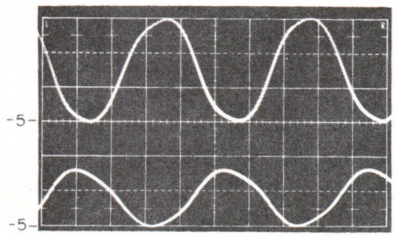




A. Top: Q26 base (EE)
Bottom: Q26 base (PB)
Both: 2 ms/cm
Highband



B. Top: Q26 base
Bottom: Q25 collector
Both: 0.2 v/cm, 0.1 μs/cm
Highband, Noise Test



C. Top: Q19 emitter, .2 v/cm
Bottom: Q20 emitter, .5 v/cm
Both: .02 μs/cm
Highband Standards

Figure 83—FM Input Amplifiers and Limiters, Schematic Diagram and Typical Waveforms

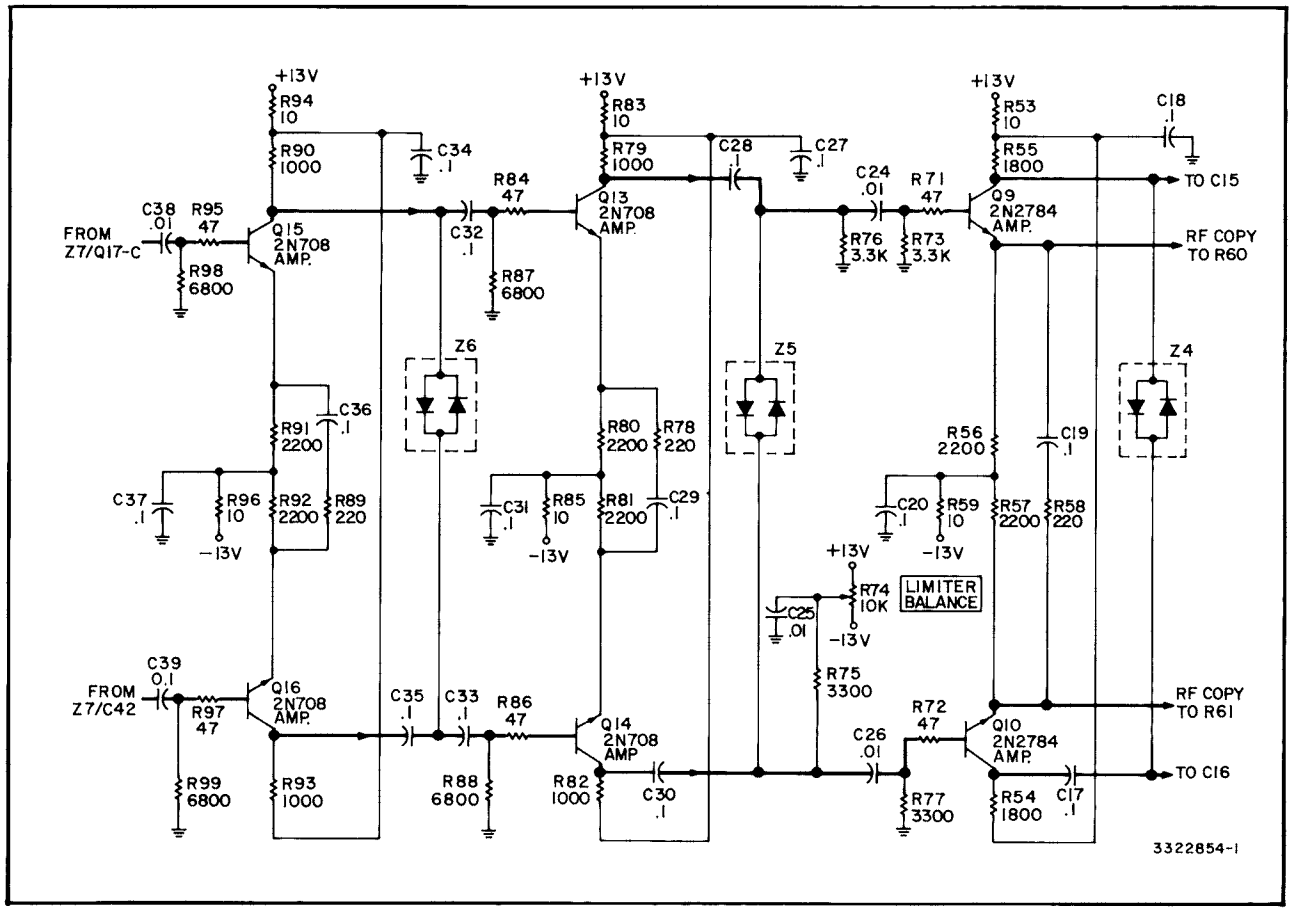


Figure 84—Amplifiers and Limiters, Schematic Diagram

transistor Q26. Resistor R130 is the emitter resistor for transistor Q25 as well as part of the collector load for Q26.

Both outputs from complementary push-pull emitter follower Q25/Q26 are of low impedance because of the multiple feedback paths and because each output is driver by a respective emitter. Outputs are coupled through capacitors C51 and C50 to their respective succeeding stages.

Amplifiers and Limiters

Five stages of amplification and limiting are used to provide precisely symmetrical square waves from the incoming FM. See figures 83 and 84. In the first stage, transistors Q21/Q23 and Q22/Q24 are differential cascode amplifiers that increase the level of their respective input signals from the phase splitter. The cascode amplifiers operate in push-pull with the limiting diodes in Z8 to form the first amplifier and limiter stage.

The cascode amplifiers are ac-coupled together by capacitor C48. Resistor R117, in combination with collector-load resistors R118 and R121, establishes the available gain of the first amplifier stage prior to limiting through Z8. Resistor R121 with inductor L8 provides the collector load for amplifier Q21/Q23. The same is provided with R118 and L7 for Q22/Q24. The small collector-load resistors and their associated peaking coils assure flat frequency response and constant delay throughout the required bandwidth.

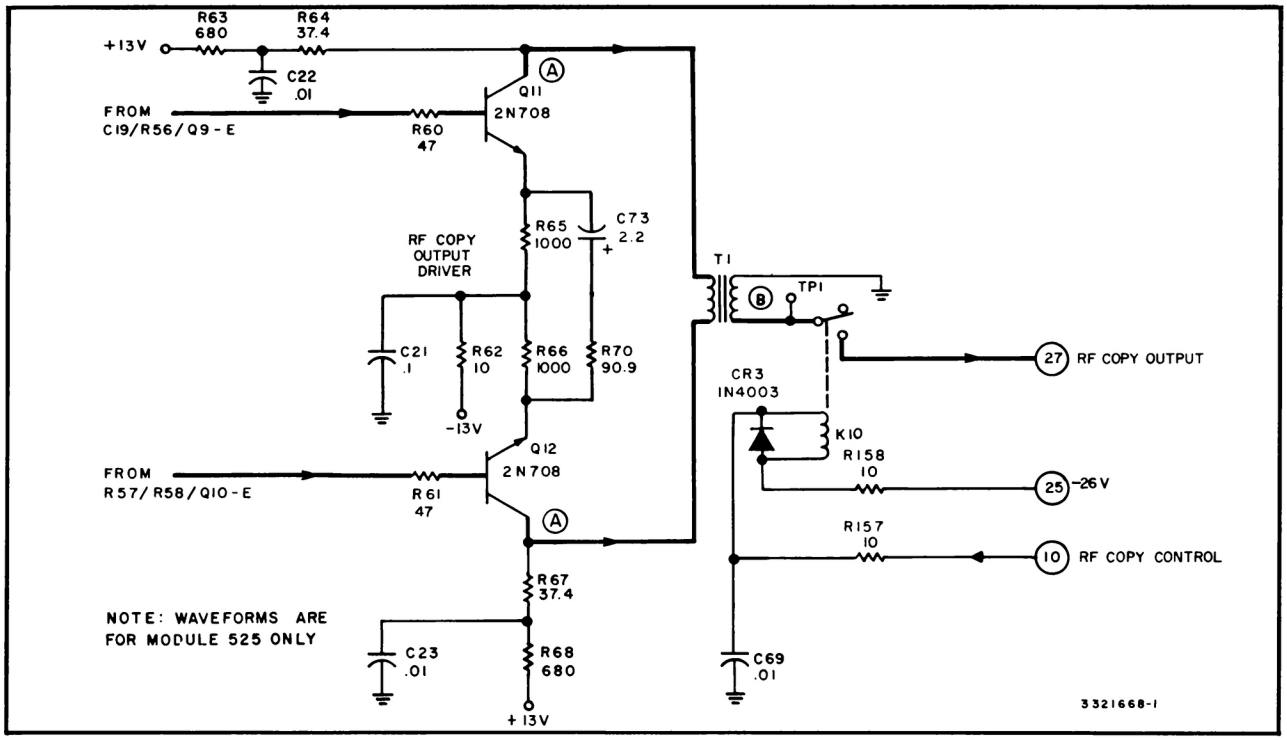
Limiting is accomplished by the two diodes that comprise Z8. The diodes conduct alternately as the signals on the collectors of Q21 and Q22 swing alternately positive and negative beyond the conduction voltage of the diodes. With a normal input level, the resultant signal from the first limiter stage is a train of square waves with zero-axis crossings corresponding to axis crossings of the input signal.

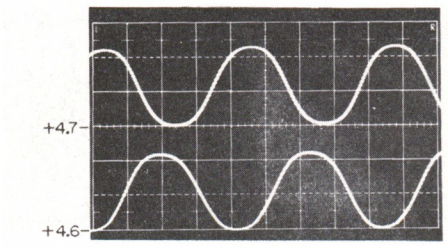
If the input signal level decreases because of head-to-tape disturbances, clipping through limiter Z8 becomes less pronounced. If the input is sufficiently low, Z8 will cease to conduct. The first limiter stage then operates simply as an amplifier to drive the limiter that follows, where initial clipping is performed.

After limiting the signal through Z8 (or plain amplification in Q21/Q24 if the signal is low), the collector output from the first stage is ac-coupled through capacitors C44 and C45 to the bases of emitter followers Q19 and Q20, respectively. The emitter followers then drive the second limiter amplifier which operates in a manner similar to the first stage. However, no shunt peaking is provided because this stage is continuously clipping. Coupling through capacitor C41 and resistor R100 controls the gain of the differential amplifier, as in the first stage.

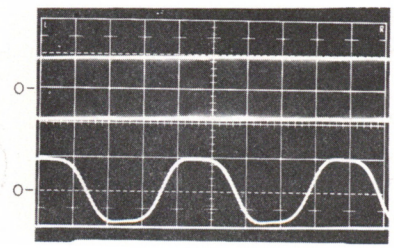
The third, fourth and fifth amplifier and limiter stages function in a manner similar to the first and second stages. However, because these stages are continously limiting heavily, wide bandwidth as in the first stage is of less importance. Each amplifier stage is coupled through its respective ac-coupling and resistor between emitters, as in previous stages.

LIMITER BALANCE potentiometer R74 controls the symmetry of the signal developed across diodes Z5. See figure 84. This is accomplished by applying a positive or negative bias voltage from the center arm of R74. The bias causes one diode to conduct sooner than the other, and because of finite rise and fall times of the signal, the symmetry of the output signal may be adjusted for exactly 50 percent duty cycle.





A. Top: Q11 collector
Bottom: Q12 collector
Both: .2 v/cm, .02 μs/cm
Highband Standards,
PLAY mode



B. Top: TP1, multiburst
Bottom: TP1, test
Both: .5 v/cm, .02 μs/cm
Highband Standards,
PLAY mode

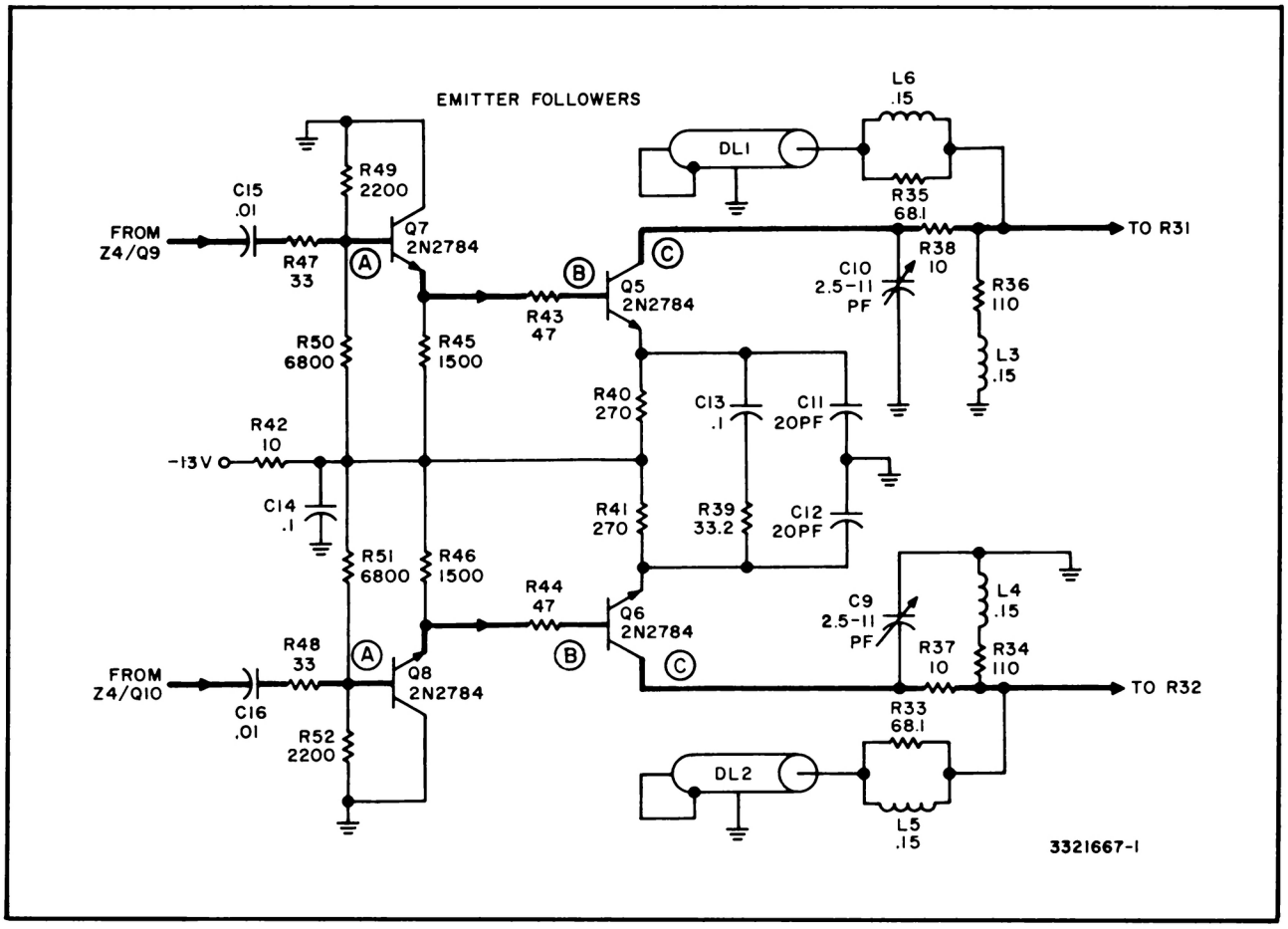
Figure 85—RF Copy Amplifier and Output, Schematic Diagram and Typical Waveforms

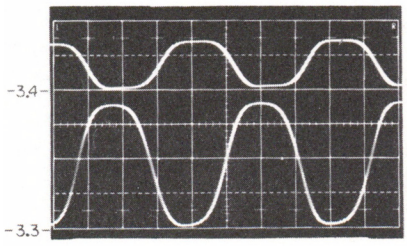
RF Copy Amplifier and Output

The rf copy output signal is taken from the fifth limiter stage, at the emitters of transistors Q9 and Q10. This signal is direct-coupled through resistors R60 and R61 to the push-pull amplifier stage (Q11, Q12), that is used to drive the rf copy output transmission line. See figure 85.

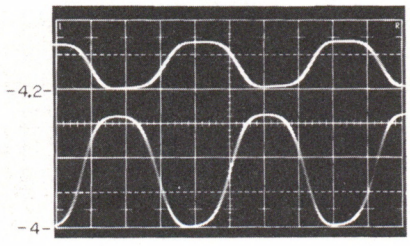
The collector outputs from push-pull transistors Q11 and Q12 are supplied to the primary winding of transformer T1. The secondary winding of T1 supplies the signal in a single-ended manner to the contacts of relay K10. Transformer T1 has a unity-turns ratio so that the 75-ohm primary termination (R64 in series with R67) is reflected into the secondary as a 75-ohm rf copy output impedance.

When the machine is operating with rf copy output, relay K10 is energized, and the limited FM signal leaves the module through pin 27 and is fed

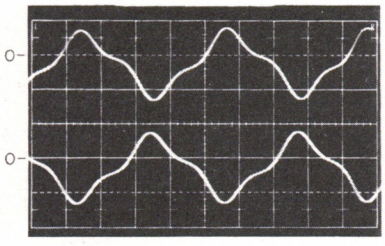




A. Top: Q7 base, .5 v/cm
Bottom: Q8 base, .2 v/cm
Both: .02 μs/cm



B. Top: Q5 base, .5 v/cm
Bottom: Q6 base, .2 v'cm
Both: .02 μs/cm



C. Top: Q5 collector
Bottom: Q6 collector
Both: 1 v/cm, .02 μs/cm

All waveforms in PLAY mode.

Figure 86—Drivers and Delay Lines, Schematic Diagram and Typical Waveforms

from the Demodulator module to a connector on the machine connector panel.

Delay Lines and Drivers

Output from the fifth and final stage of the limiter is ac-coupled from the collector of Q9 through capacitor C15 and resistor R47 to the base of Q7. The opposite phase is through capacitor C16 and resistor R48 to the base of Q8. Transistors Q7 and Q8 are emitter followers that further couple the signals to differential amplifier transistors Q5 and Q6. Dc bias on these stages is established by the voltage divider consisting of resistors R49, to R52, between minus 13 volts and ground. See figure 86.

Operation of the two delay lines is similar, therefore only that using transistors Q5 and delay line DL1 is described. The collector of Q5 develops a square-wave collector current in accordance with the square-wave voltage drive on its base. When the base begins to follow a positive-going transition, the increased collector current through load resistor R36 causes the collector voltage to drop. The negative-going transition thus developed across resistor R36 and peaking coil L3 is propagated down the shorted transmission line.

At the conclusion of the transition, the collector voltage of Q5 is maintained at a negative level until the wave initially propagated through delay line DL1 is reflected. This reflection is out of phase with the original negative transition and will therefore cancel the negative potential at the collector of Q5. The length of the transmission line is such that 17 nanoseconds are required for a transition to travel up the line, be reflected, and return out of phase to the input of the line. A similar effect occurs for negative base voltage transitions, except that all signals polarities are reversed. See waveforms on figure 87.

Another manner of understanding this circuit is to consider the collector of Q5 to be short circuited by the shorted delay line (which is in fact a dc short circuit) except during the interval required for a change in level to be propagated down and back through the line. This is a 17 nanosecond interval, and the collector of Q5 is permitted to be at other than ground level during this interval.

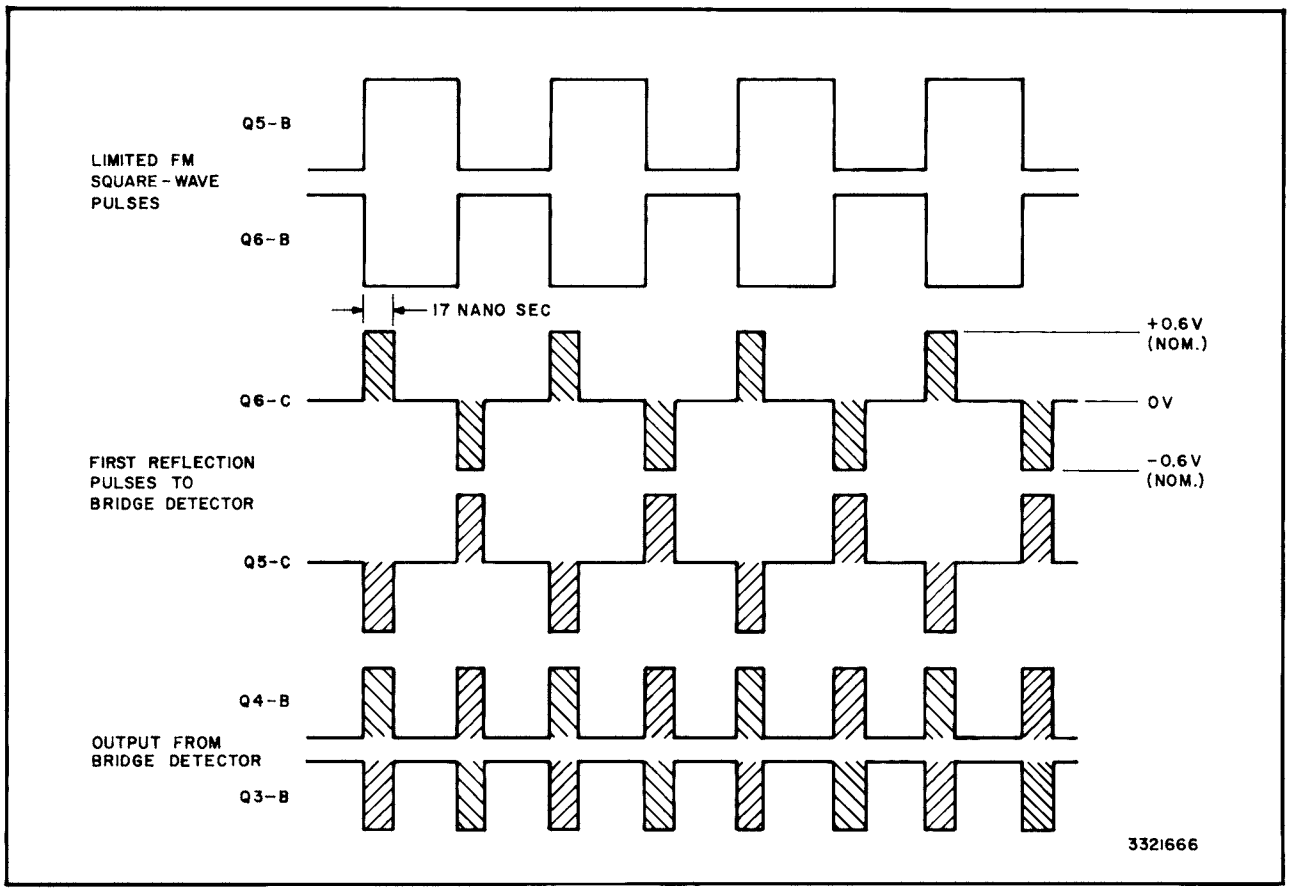
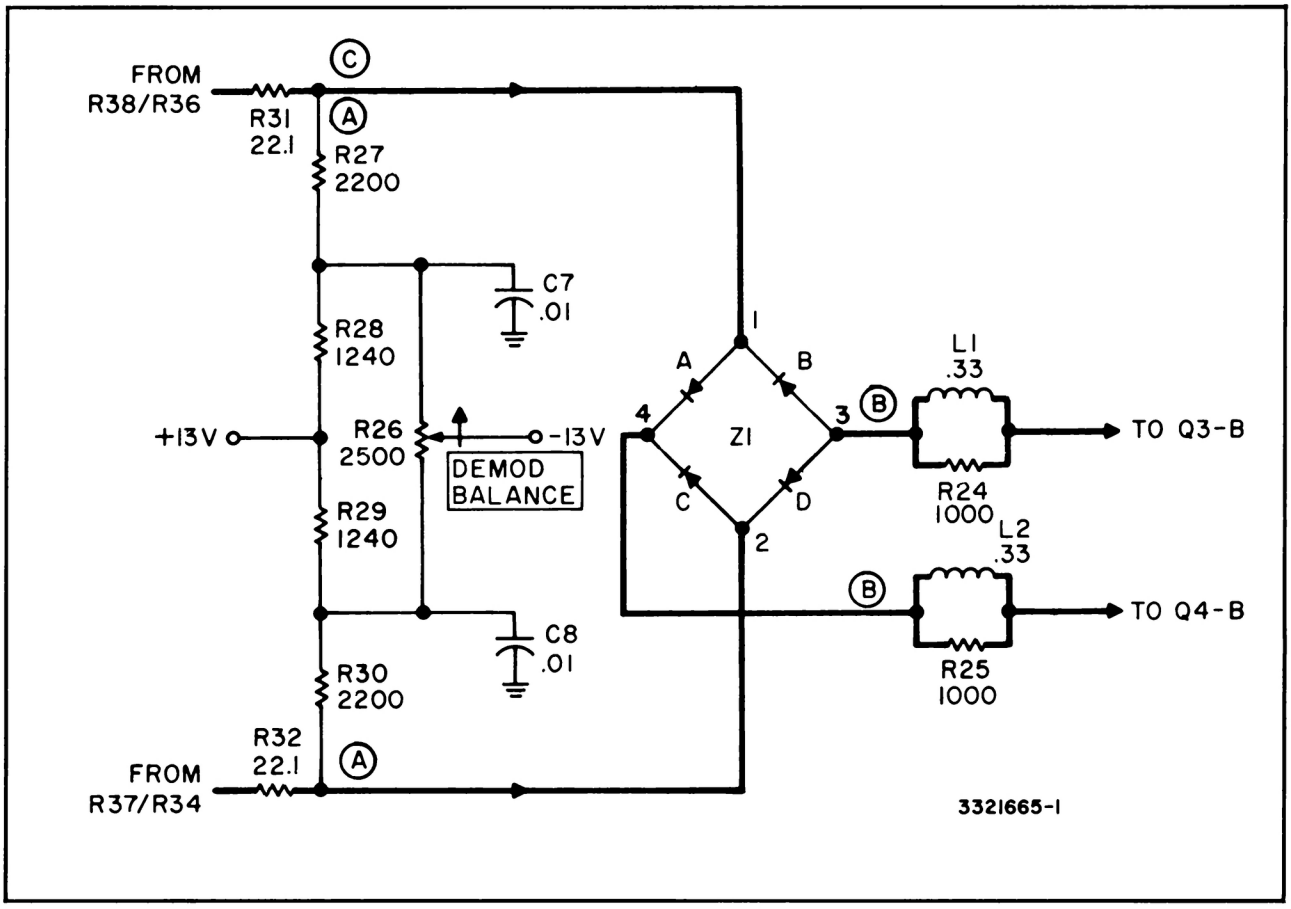
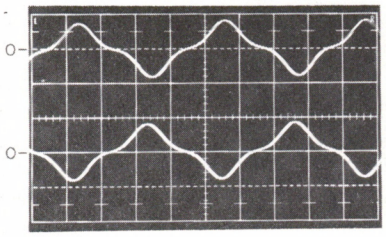
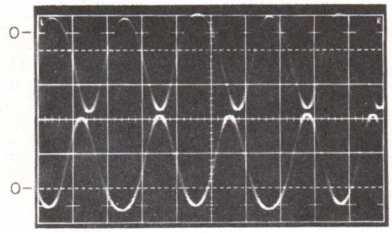


Figure 87—First Reflection Pulses Supplied to Delay Lines, and Bridge Detector Output Waveforms

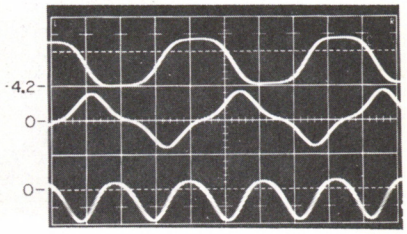




A. Top: Junction Z1/R27
Bottom: Junction Z1/R30
Both: 1 v/cm, .02 μs/cm



B. Top: Junction Z1-3/L1
Bottom: Junction Z1-4/L2
Both: 1 v/cm, .02 μs/cm



C. Top: Q5 base, .5 v/cm
Middle: Junction Z1/R27, 1 v/cm
Bottom: Q3 base, .5 v/cm
All: .02 μs/cm

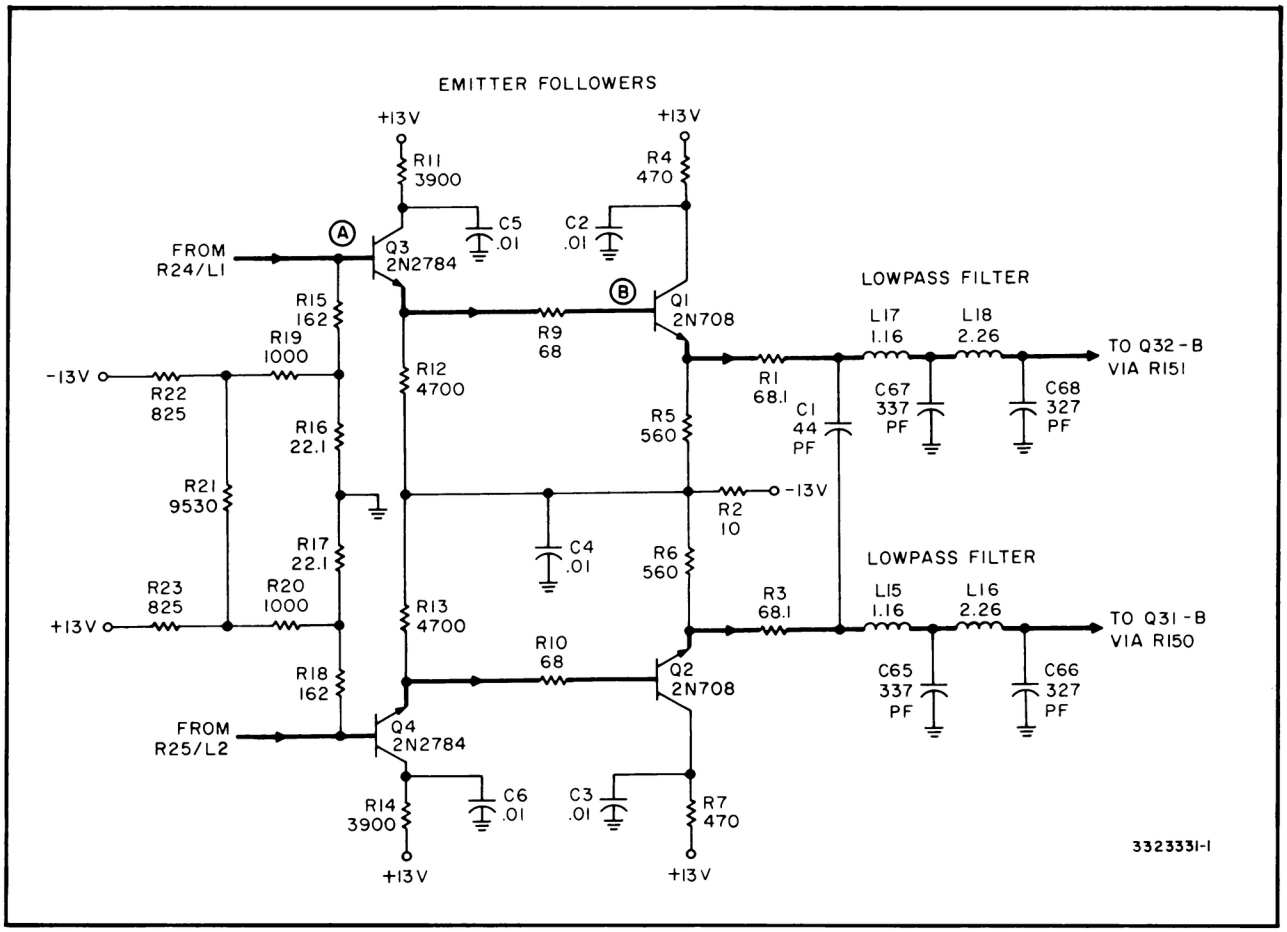
All waveforms in PLAY mode.

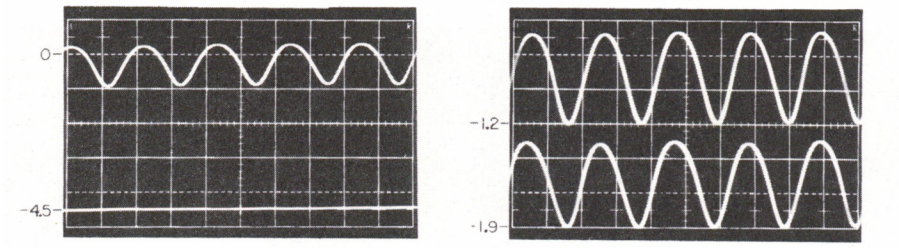
Figure 88—Diode Detector, Schematic Diagram and Typical Waveforms

With the above described conditions, a 17-nanosecond pulse is created at the collector of Q5 for each square-wave transition of the base of Q5. Coupling between the halves of the differential amplifier is through capacitor C13 and resistor R39. Capacitors C11 and C12 peak the high frequency response, and capacitors C9 and C10 provide variable response rolloff to minimize pulse distortion. The RL network using R35 and L6 at delay line DL1, and R33 and L5 at DL2 are used to precisely match the cable impedance.

Diode Detector

Alternate positive and negative 17-nanosecond pulses are fed from one side of the push-pull circuit to input 1 of the diode detector bridge (Z1). Simultaneously, pulses 180 degrees out of phase are fed from the opposite phase of the push-pull circuit to input 2 of the diode detector bridge. The quad diodes in Z1 function as a bridge rectifier pulses to specific outputs. Positive pulses from both inputs are transferred to output 3, and negative pulses from both inputs appear at output 4. See figure 87.





A. Top: Q3 base
Bottom: Q3 collector (dc)
Both: .5 v/cm, .02 μs/cm

B. Top: Q1 base
Bottom: Q1 emitter
Both: .2 v/cm, .02 μs/cm

All waveforms in PLAY mode.

Figure 89—Emitter Followers and Low Pass Filters, Schematic Diagram and Typical Waveforms

DEMOD BALANCE potentiometer R26, in conjunction with resistors R28 and R29 form a voltage divider between plus 13 volts and minus 13 volts. The dc level and polarity across bypass capacitor C7 may be changed relative to the level at capacitor C8 by adjusting potentiometer R26. These dc potentials are coupled through resistors R27 and R30 to the two diode-bridge inputs to control the average conduction level of the diodes. This permits balancing the amplitudes of the alternate positive output pulses alternate negative output pulses. Refer to figure 88.

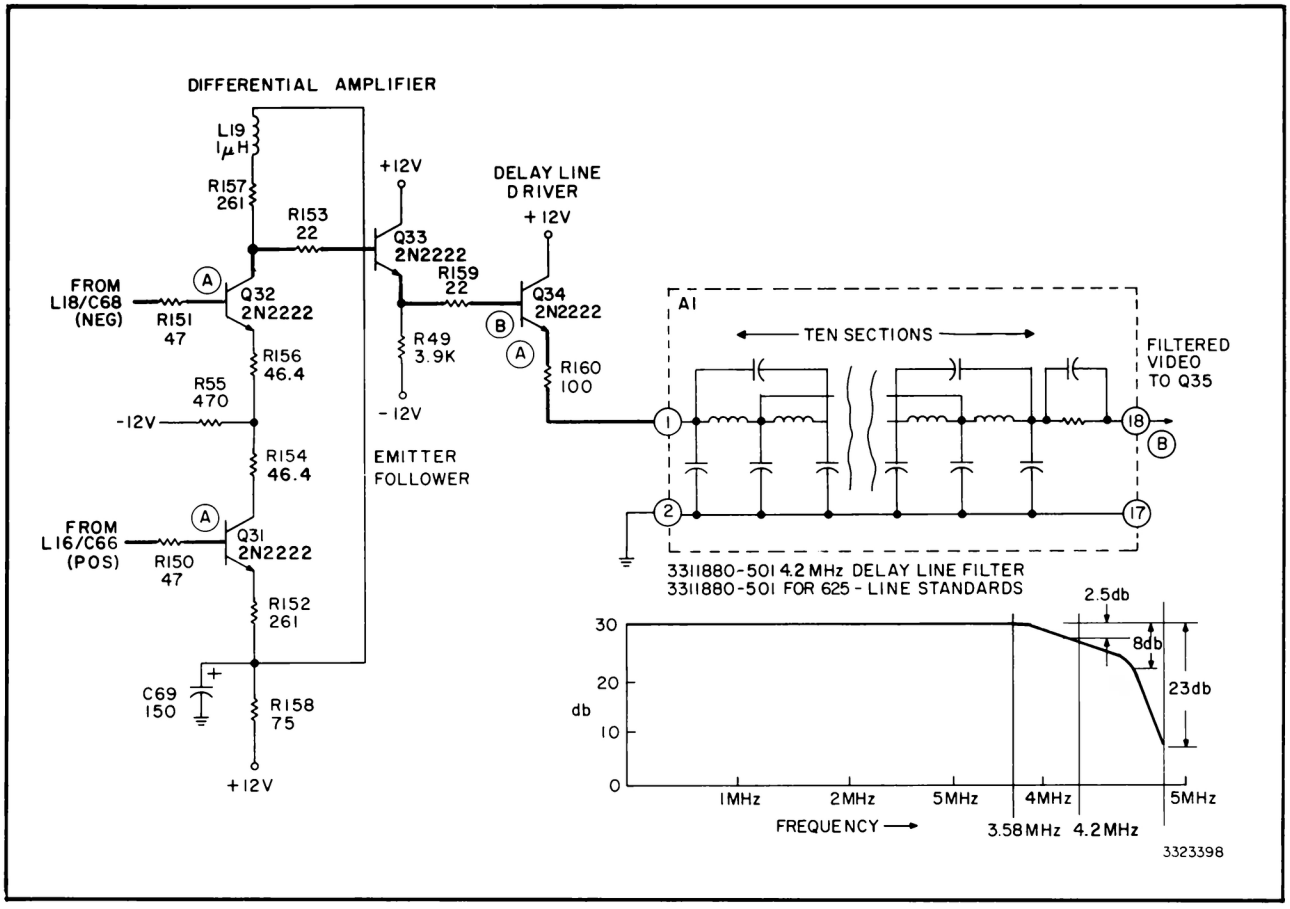
Emitter Followers and Low Pass Filters

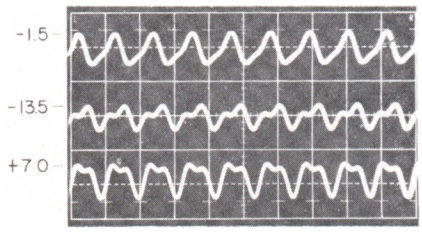
Detected, but unfiltered, the signal supplied from the diode bridge is fed to two emitter followers in series. The positive pulses are fed to the base of Q4 and the negative pulses are fed to the base of Q3. Dc bias is developed for the bases of Q3 and Q4 by the network consisting of resistors R15 through R23. A somewhat positive bias applied to the base of Q3 centers the positive signal at that point in the amplifier-operating range. A slightly negative bias is

applied to the base of Q4 for a similar purpose. See figure 89.

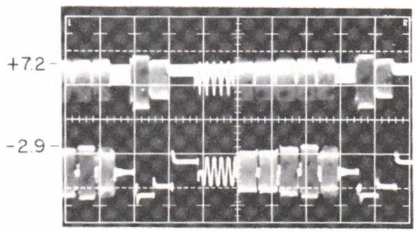
Transistors Q2 and Q4 are emitter followers that operate in series and supply the positive pulses to the lowpass filter network through termination resistor R3. Transistors Q1 and Q3, likewise, supply the negative pulses to the lowpass filter network through resistor R1. These emitter followers provide a low impedance to the input of the lowpass filters. Resistors in series with the transistor collectors reduce dissipation in the emitter followers and provide decoupling.

The lowpass filters have a flat bandpass characteristic in the normal video range but attenuate to a considerable degree FM products above the video spectrum. Positive pulses were fed to the filter section driving the base of Q31; therefore, as the Modulator module frequency increases because of white-going video information, the rate of positive energy input increases and reproduces video at the filter output





A. Top: Q32 base, 0.05 v/cm
Middle: Q31 base, 0.05 v/cm
Bottom: Q34 emitter, 0.2 v/cm
All: 0.1 μs/cm
Noise Test



B. Top: Q34 emitter, 1.0 v/cm
Bottom: Q35 collector, 0.5 v/cm
Both: 10 μs/cm

Figure 90—Differential Amplifier and Filter, Schematic Diagram and Typical Waveforms

with white positive-going video. Similarly, because negative pulses are fed to the opposite filter section, the output from that section (driving the base of Q32) will become progressively more negative as the carrier increases in white-going circumstances. The output signal from the filters is a mixture of video (as recovered in the demodulation process) and remnants of the positive and negative pulses that are now partially integrated.

Differential Amplifier

The partially-filtered signal from the lowpass filters is supplied to the differential amplifiers, Q31, Q32, that supplies a combined output to the delay line filter. The signal derived from positive pulses is fed to one input of the differential amplifier using transistor Q31. The opposite, partially-filtered signal derived from negative pulses is fed to the other input of the differential amplifier using transistor Q32. See figure 90.

Since the differential amplifier measures the difference between the two signals at its base elements, the output from the collector of Q32 is the sumation of the positive and negative input pulses. Any in-phase frequency component in the input signals will be cancelled out by the action of the differential amplifier.

The output at the collector of Q32 is fed through resistor R153 to the base of emitter follower Q33. Transistor Q33 provides the current to drive the delay line driver transistor Q34. The output from the emitter follower delay line driver Q34 is applied to the input of the appropriate filter, which is terminated at both ends in 100 ohms. A 4.2 MHz filter is used on 405-525-line standards, whereas, a 5 MHz filter is used on 625-line standards.

The filter, in either case, is designed to eliminate all frequencies above the video band, and deliver at the output a varying average dc whose amplitude changes are a function of the video frequency modulated input. The result of this is an output signal that is a replica of the video signal initially applied to the recorder. As mentioned earlier, the discriminator output frequency is twice that of the input. The purpose of frequency doubling is to facilitate the separation of the video and the carrier components in the filter, since with some standards the spectra of the two signals overlap. In other words, the carrier frequency, which represents the sync and blanking region, may extend down into the filter bandpass, overlapping the video component. By using the frequency doubling technique prior to filtering, such a condition is avoided. Asymmetry, whether present in the FM signal from the limiter stages or caused by unbalance in the discriminator diodes, will introduce an unwanted component of the carrier fundamental frequency into the filter. In addition to the desired carrier frequency, this unwanted component may be within the bandpass range of the filter and, therefore, fail to be eliminated from the video output of the filter.

The filter is constructed of 10 pi-type filters with bridging capacitors that produce an output characteristic curve similar to that shown on figure 90. The output of the filter is fed to the common base amplifier Q35.

Video Amplification and Post Emphasis

Filtered video from the delay line filter is supplied to the emitter of Q35 where the signal is amplified to a level suitable for driving the next stage. Shunt high frequency compensation is provided by inductor L20. Use of a variable inductor in the high frequency compensation network enables the pass band at the high end to be adjusted for a flat response. See figure 91.

The output of Q35 is fed to emitter follower Q36 which provides isolation, and its output is supplied to the video feedback amplifier Q37, Q38. Amplified video at the collector of Q38 is fed to emitter follower Q39 which provides the current gain to drive the post emphasis circuits.

The post emphasis circuits are made of relays K5 to K9 and RC networks. An RC network is connected to each relay between the center arms of the two sections of the relay contacts. Only one of these RC networks is connected in series with the video signal path by energizing the relay associated with that network. The selected network is driven by resistor R204 and terminated by the resistor in the input circuit on the Demodulator Output module.

Each post emphasis RC network consists of a "T" network having an RC shunt arm, as shown on figure 91. At low frequencies, the capacitive reactance of the network is so high that capacitor C86 is ineffective and only resistors R191 and R192 are effectively in the circuit. The resistors in series with the terminations thus determine the video level supplied to the subsequent amplifier, and thereby set the low frequency playback gain according to the standards selected. The relative playback gain for the various standards are tabulated in table 8.

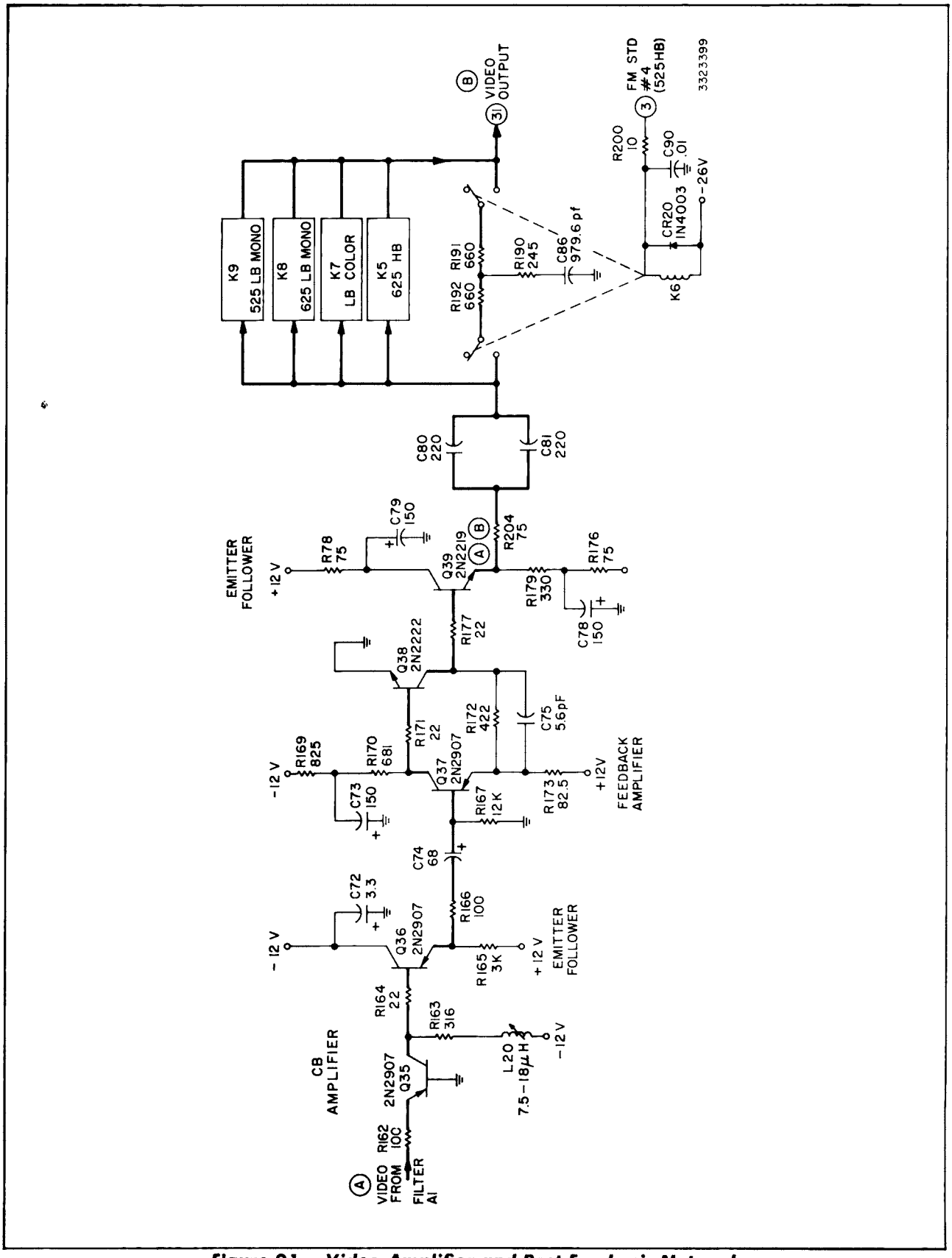
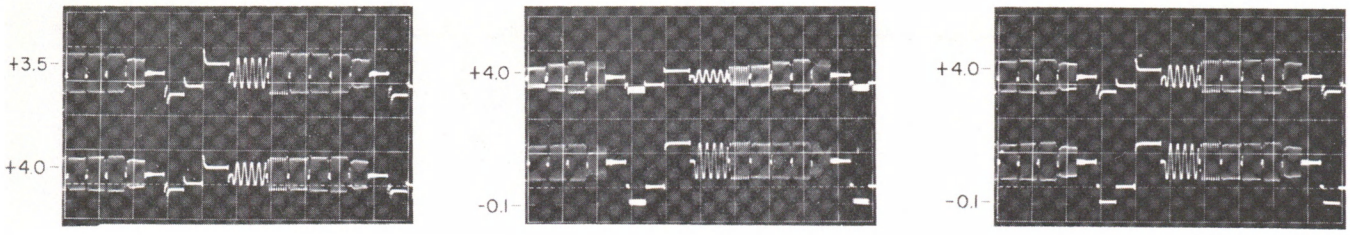


Figure 91—Video Amplifier and Post Emphasis Network, Schematic Diagram and Typical Waveforms



A. Top: A1 FILTER OUTPUT, 0.2 v/cm
Bottom: Q39 emitter, 5 v/cm
Both: 10 μs/cm

B1. Top: Q39 emitter, 5 v/cm
Bottom: P1 pin 31, 0.1 v/cm
Both: 10 μs/cm
LB Mono

B2. Top: Q39 emitter, 5 v/cm
Bottom: P1 pin 31, 0.1 v/cm
Both: 10 μs/cm
HighBand

Waveforms in PLAY mode.

Figure 91—Video Amplifier and Post Emphasis Network, Schematic Diagram and Typical Waveforms (Continued)

TABLE 8—POST EMPHASIS STANDARDS SELECTIONS

Function	*STANDARDS*				
	1 *405/525* *LB Mono*	*2* *625* *LB Mono*	*3* *525* *LB Color*	*4* *405/525* *HB*	*5* *625* *HB*
POST EMPHASIS A_{LF}/A_{HF} 1.	1/.2	1/.333	1/.132	1/.4	1/.4
RELATIVE LF TRANSMISSION 2.	1.0	1.429	3.57	0.869	1.25
POST EMPHASIS (−3 dB @ LF GAIN)	1.3 MHz	1.2 MHz	0.7 MHz	0.35 MHz	0.35 MHz
RELAY ACTIVE	K9	K8	K7	K6	K5

1. A_{LF}/A_{HF} is ratio of gain at low frequency to gain at maximum rolloff frequency.
2. Relative transmission for standards 2 and 5 are referenced to standard 1. Absolute levels are related to low frequency deviation.

As the video frequency increases, the capacitor in the post emphasis network becomes more effective in decreasing the impedance of the shunt arm of the "T" network. Finally, at the highest operating frequencies, resistor R190 is essentially connected directly to ground. Thus, at high frequencies, the video output level is determined by the attenuation of the "T" network consisting of R191, R192 and R190, and is considerably lower than at lower video frequencies during which time the shunt arm has not effect. The ratio of low frequency-to-high frequency level for each standard is listed as A_{LF}/A_{HF} in table 8, and is a measure of the demodulated video signal. Post emphasis of the video signal becomes effective as determined by the capacitor value and the relationship of its reactance-to-circuit resistance.

One terminal of each post emphasis relay coil is connected to −26 volts. The opposite coil terminal of each relay is connected to one of five standards buses as supplied from the Standards Generator module. Selection of a given operating standard connects ground to a corresponding standards bus through the Standard Generator module, and operates the proper relay.

Post emphasized video from the selected RC network is directly connected to the output, pin 31, to the Demodulator Output module.

FM Standards Selector Switch

The FM standards selector switch, S1, is located on the front panel of the Demodulator module. It is a three position two wafer rotary switch. See figure 111 and figure 112 in the Standards Generator module description. In position 1, the A section is not functional. The B section, however, applies ground potential to the Standards Generator module where it activates relays K1 or K2 depending on the condition of the special VI and VN buses. The ground con-

nection also completes the circuit to light the LB MONO indicator.

When the switch is in position 2, the A section provides a potential to the NON-STD indicator. This lamp lights whenever the VN bus is at ground which indicates that a non-standard selection has been made. When the VN bus is at −26 volts, then the lamp goes out. Section B provides a ground potential to the Standards Generator module where it activates relay K3 whenever the VN bus is at −26 volts. The ground connection also completes the circuit to light the LB COLOR indicator.

When the switch is in position 3, the A section is not functional. The B section, however, applies ground potential to the Standards Generator module where it activates relays K4 or K5 depending on the condition of the special VI and VN buses. The ground connection also completes the circuit to light the HB indicator on TR-22 High Band machines.

ADJUSTMENTS

The Demodulator module has been carefully adjusted at the factory with special test equipment and should not be disturbed. All adjustments have been locked to their proper settings with red or blue sealing compound. If service is required, contact your RCA field representative.

DEMODULATOR OUTPUT MODULE

CIRCUIT DESCRIPTION

General

The Demodulator Output module is a double width module with two circuit boards. Board 1 contains the output amplifiers for the post-emphasized video signal from the Demodulator module, and a sensor circuit which determines whether the quality of the tape video signal is good enough to permit automatic operation of the guide servo system (TR-22HB only), and provides a control signal which switches the guide servo to manual operation when the quality is unacceptable. Board 2 contains a clamped sync separator which provides sync to the sensor circuit on board 1, the headwheel servo system, and to the monochrome ATC system. Since the Sync

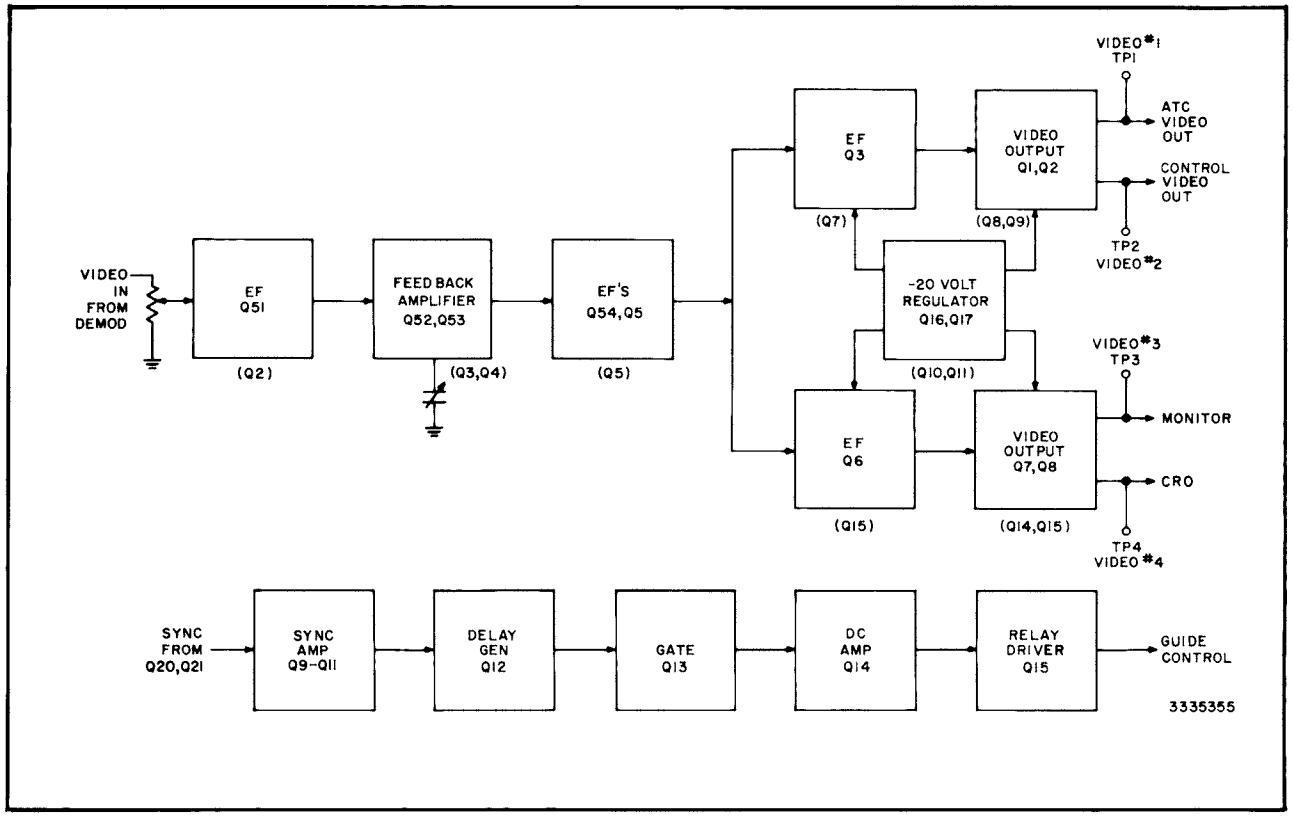


Figure 92—Demodulator Output Module Block Diagram, Video Out and Guide Servo Control (TR-22 Only)

Separator on Board 2 is adequately described in Instruction Books already provided with the Recorder, the information is not repeated here.

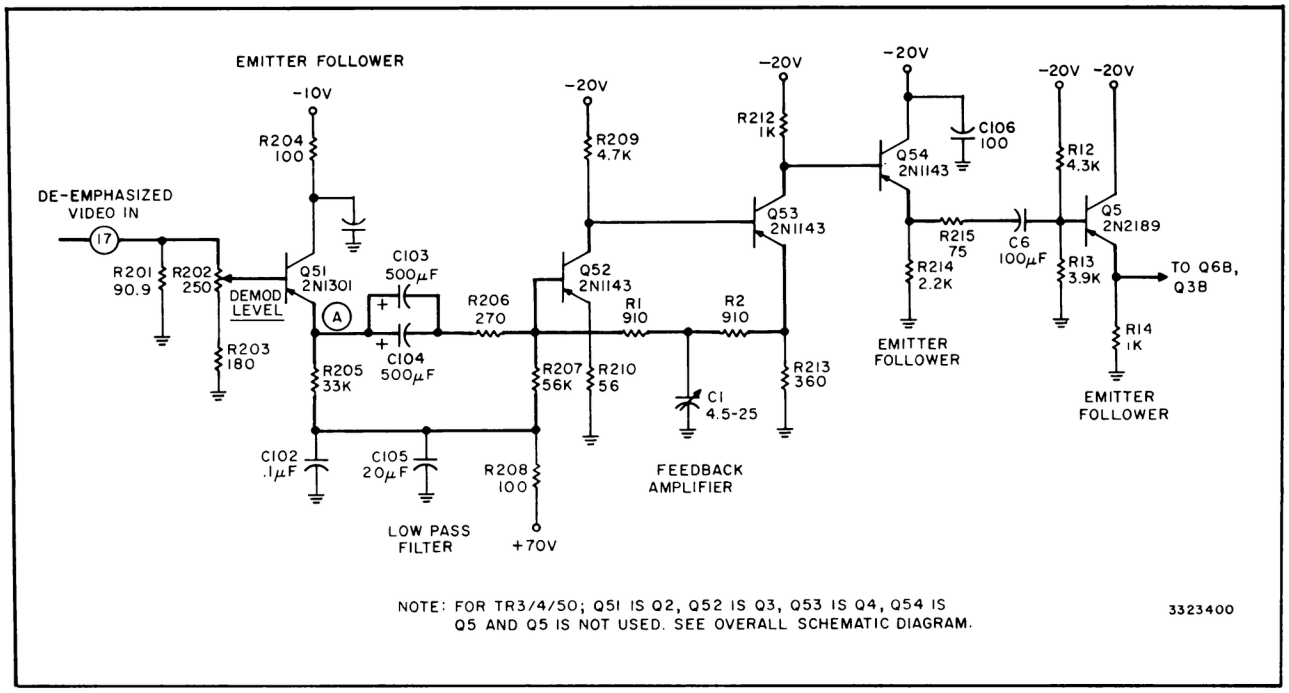
NOTE: The basic description of this module covers all the high band machines. Wherever possible, reference to the TR 3/4/50 machines are made, but the detailed description covers the TR22 machine.

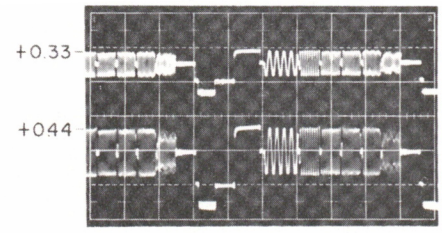
VIDEO OUTPUT AMPLIFIER CIRCUITS, BOARD 1

While reading the following circuit descriptions, refer to the block diagram, figure 92, and the simplified schematics. Components in parentheses indicate the symbol number used for TR-3/4/50 tape equipment.

The video output amplifier section of the Demodulator Output module amplifies the video signal from the Demodulator module and provides four video outputs. The first video output goes to the input of the monochrome ATC system, which is the Fixed Delay Line, FDL1. The second output is not used. The third video output goes to the picture monitor, and the fourth to the CRO waveform monitor.

The circuit of the video output section (see figure 93), consists of an input emitter follower, Q51 (Q2), feedback amplifier Q52, Q53 (Q3, Q4) and emitter follower(s) Q54, Q5 (Q5) which feeds two amplifiers chains. One amplifier consists of an emitter follower, Q6 (Q13) followed by a series line driver, Q7, Q8, (Q14, Q15). The other section consists of an emitter follower Q3, (Q7) and a series line driver, Q1, Q2 (Q8, Q9). The emitter follower and line driver are identical to those in the first section, therefore, only one amplifier section shall be described.





A. Top: Q51 emitter, 0.1 v/cm
Bottom: TP1, 0.5 v/cm
Both: 10 μs/cm
PLAY mode

Figure 93—Video Amplifier, Schematic Diagram and Typical Waveforms

Video Input

The 2-volt post-emphasized video signal from the output of the Demodulator module is fed through P1-17 and potentiometer DEMOD LEVEL, to the base of the input emitter follower. See figure 93. The output of this stage is fed through the two 500 microfarad capacitors to the base of the feedback amplifier. The capacitors and R208 in the lower portion of the emitter is a decoupling network of the +70 volt input. The feedback amplifier has a peaking circuit to compensate for any frequency attenuation through the video amplifier. The video signal from the feedback amplifier is directly coupled to the emitter follower stage and then ac coupled to emitter follower Q5. From the emitter of Q5 the video signal is fed to the two identical video amplifier sections.

Video Distribution

The output of emitter follower Q6 is fed to the base of one of the two transistors, Q7, in the series line driver. The signal from the collector of Q7 is applied through capacitor C7 to the base of Q8. A Zener diode CR2, provides a constant voltage difference of 12 volts between the collector of Q7 and the base of Q8. The output of the line driver is taken from the junction of the emitter of Q7 and the collector Q8. Thus the circuit can be considered to be an emitter follower, Q7, with Q8 as dynamic emitter load, or a common emitter amplifier, Q8, with Q7 as a dynamic collector load.

The output of Q7 and Q8 is fed to two paths. The two go through individual resistors and capacitors, via P1-29 and P1-30, to the picture monitor and CRO respectively. The capacitors provide dc isolation, and the resistors provide the required 75 ohm termination to the coaxial lines. These two outputs may be observed at test points TP3 and TP4 (see B, figure 94).

The video output of emitter follower Q5 is fed to a circuit consisting of emitter follower Q3, and series line driver Q1 and Q2, which is identical to the other

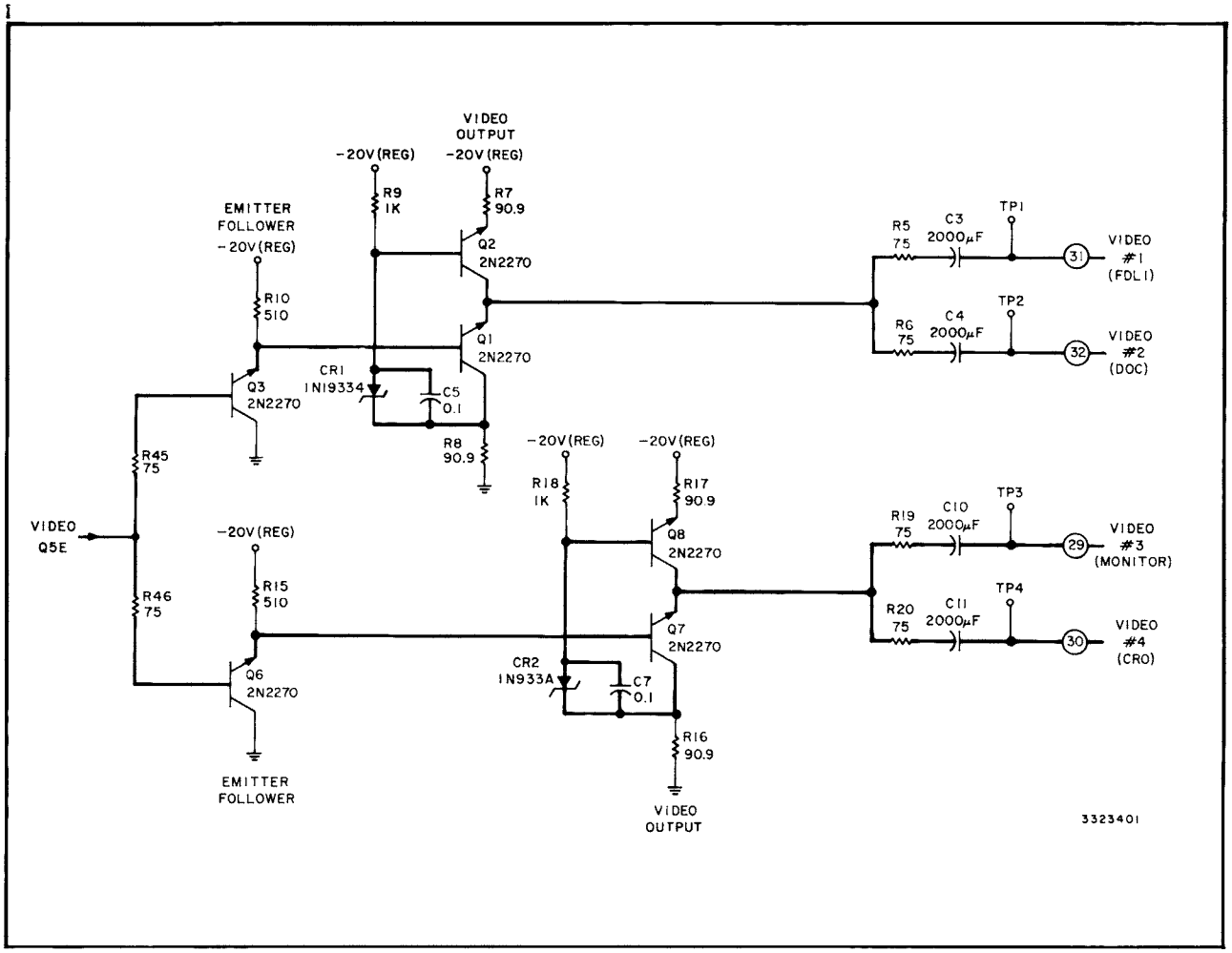


Figure 94—Video Distribution, Schematic Diagram and Typical Waveforms

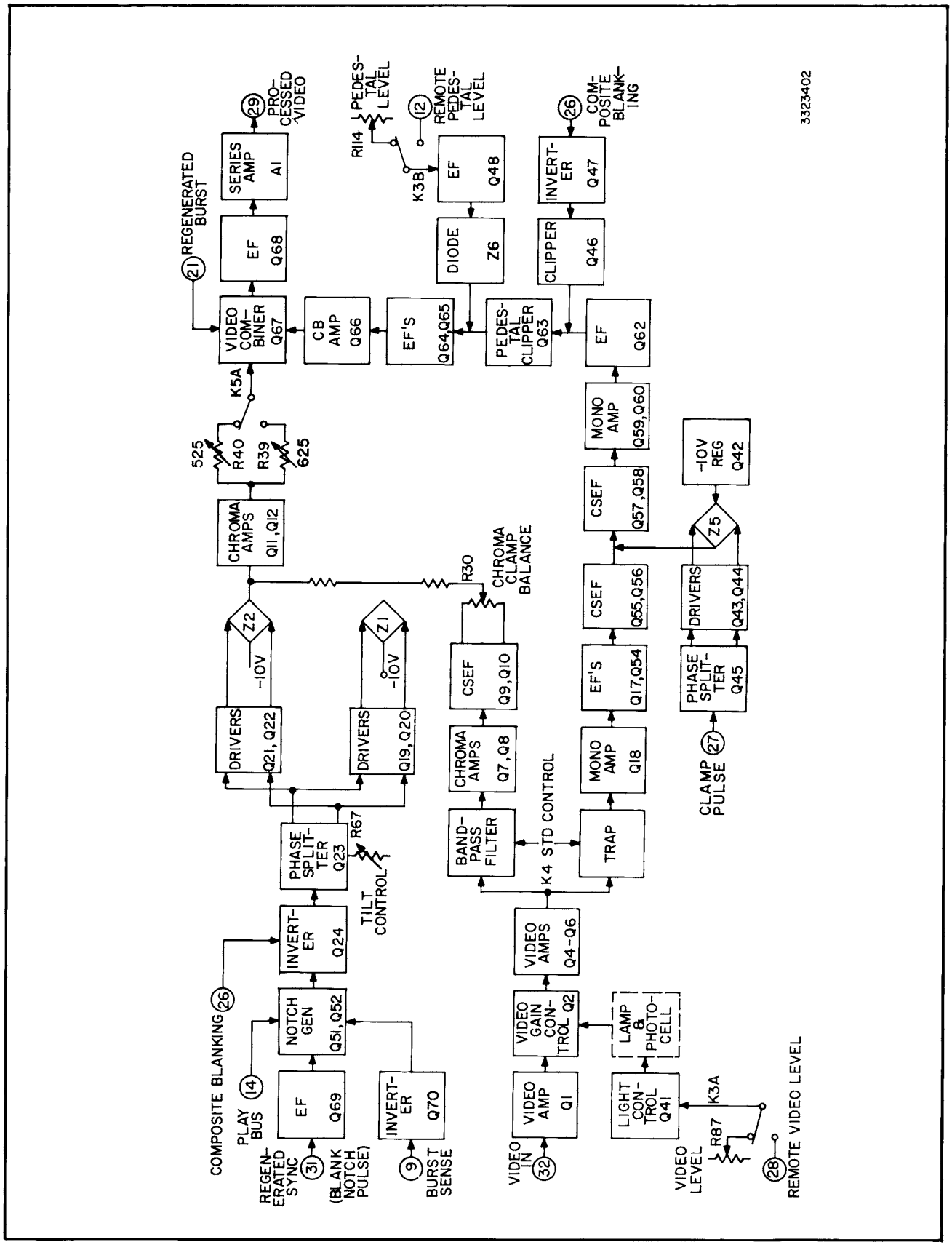


Figure 95—Video Processor Module, Block Diagram

video section. Two outputs are obtained from this section, one of which goes through P1-31 to the fixed delay line, FDL1, which constitutes the video input of the monochrome ATC system, and the other output is terminated. The two outputs may be observed at test points TP1 and TP2 (see figure 94).

Signal Sense for Guide Servo Control (TR-22HB Only)

The module contains a circuit which senses the quality of the video signal and prevents the guide servo from entering the automatic mode if sync is absent or the signal is too noisy. The circuit consists of a signal sense circuit, Q9, Q10, Q11, Q12, Q13, a dc amplifier, Q14, and a relay driver, Q15. This circuit is only available on TR-22 machines since the other machines do not have the facilities for guide control except as an accessory. Refer to instruction books provided with the machine for a description of the circuit operation.

VIDEO PROCESSOR MODULE

CIRCUIT DESCRIPTION

General

The Video Processor module provides a stabilized video signal for the Video Output module. The video signal is clamped to set the proper dc level. Input burst along with old blanking and sync is eliminated. A new and an adjustable pedestal level is inserted in the signal and regenerated burst is added.

As shown in figure 95, incoming video is fed to the video input and gain control circuit. The video output of the gain control circuit is amplified and then fed to two separate circuit branches, one chroma, the other monochrome.

At the input to each branch is a tuned circuit. The tuned circuits are designed to separate the chroma and the monochrome frequency components prior to processing. The tuned circuits complement each other in that the one in the chroma branch serves as a band-pass for frequencies in the subcarrier spectum, while the tuned circuit in the monochrome branch acts as a trap to the frequencies in the subcarrier range. Thus only the chroma frequency components appear in the video signal being applied to the chroma channel and all other frequency components appear in the video being applied to the monochrome channel.

The chrome and monochrome frequency components must be handled in different channels since the subsequent processing involves clamping, clipping and a new pedestal level. Although both signals, chroma and monochrome, require clamping, the monochrome signal, in addition, has the old pedestal level clipped and a new pedestal inserted. Clamping takes place during the back porch period; therefore if the two signals were not clamped separately in their respective channels, those portions of the chroma signal which extend below the blanking level would be eliminated. Furthermore, although the chroma clamp eliminates input burst during playback of color tape, so that regenerated burst can be added later, when the machine is in the E-E mode, regenerated burst is not available and input burst must be allowed to pass. Thus in the E-E mode input burst would be eliminated from the video signal if monochrome and chroma were not clamped separately. Therefore the monochrome and chroma frequency components are processed as separate signal entities, after which they are again combined.

The clamp potential is interposed on the chroma signal during the entire blanking interval by two clamp quads in cascade. Cascade or double clamping is required in the case of the chroma signal to insure that virtually all traces of input burst will be eliminated by the clamp potential.

In the E-E mode a slightly different situation exists with regards to input burst. The regenerated burst circuit which supplies new burst for insertion in the signal later on is disabled. Some provision must be made, therefore, to pass input burst during the clamp interval; otherwise burst will be lacking in the video output signal. Therefore a blanking notch pulse, which is derived from the trailing edge of the delayed regenerated horizontal sync pulse, is inserted in the horizontal blanking pulse.Since gating pulses for the chroma clamp quads are derived from horizontal blanking, the notch pulse causes a brief interruption of discontinuity in the normally on time of the clamp quads. Since this interruption is timed to occur during the input burst interval, the clamp quads will be turned off at this time and input burst will be able to pass. At the end of the notch pulse period, the clamp quads are again

turned on and clamping is resumed until the end of the blanking interval.

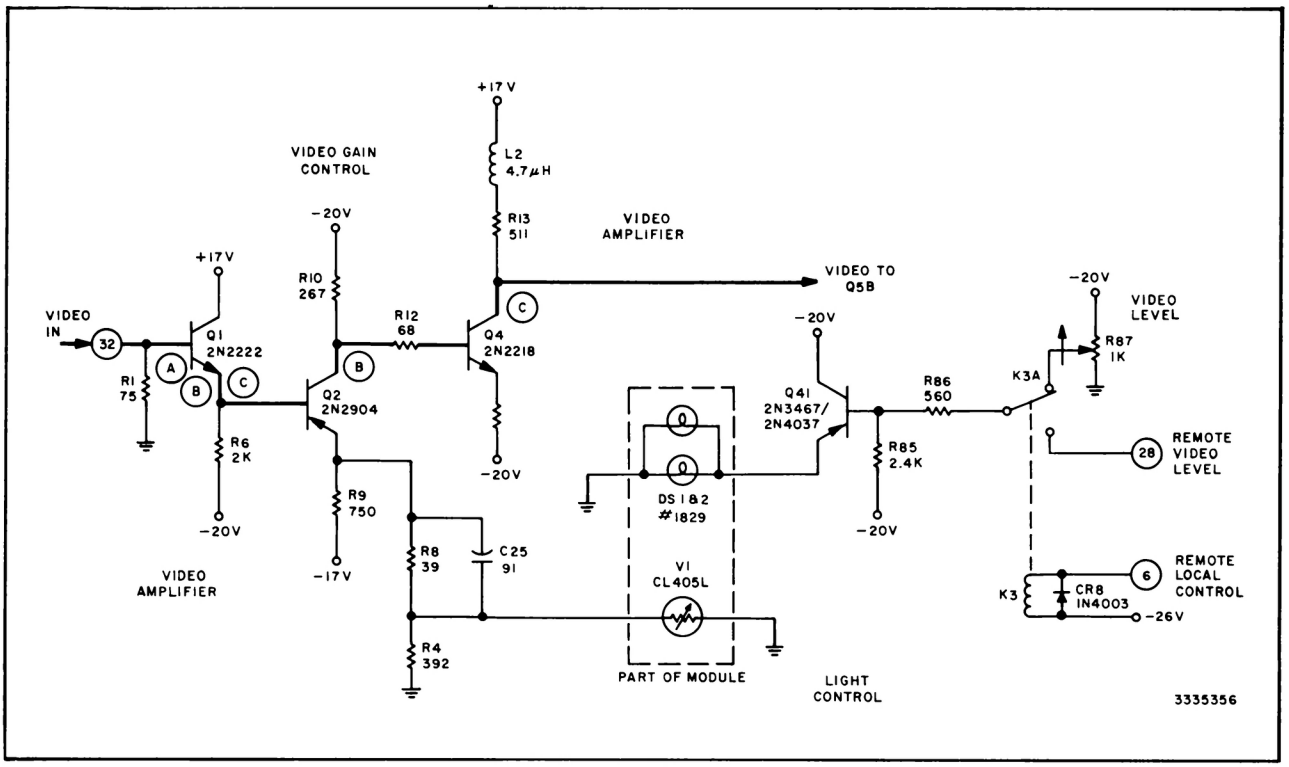
The monochrome signal is clamped during the back porch interval. The clamp potential is inserted in the monochrome signal by a clamp quad keyed on by gating pulses derived from horizontal sync. After being clamped the video signal continues to be processed. New blanking is added to the existing blanking pulse, greatly increasing the amplitude of the blanking pulse. Thus noise or switching transients present in the old blanking or sync are forced far below the normal pedestal level prior to clipping.

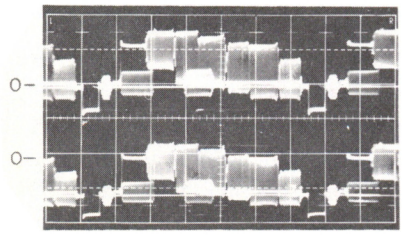
The signal is then passed across a diode clipper. Clipping takes place at the new pedestal level and all the existing blanking and sync components are eliminated. The pedestal level is established by a dc control voltage applied to the clipper diode a relay enables selection of either adjustable local or remote control of the pedestal level.

The clamped monochrome signal with a new pedestal and the clamped chroma signal are applied simultaneously along with regenerated burst to the video combiner. Here the separate signal elements are combined to form a single video signal. The video signal then goes to the video line driver which provides a low source impedance for driving the video output line.

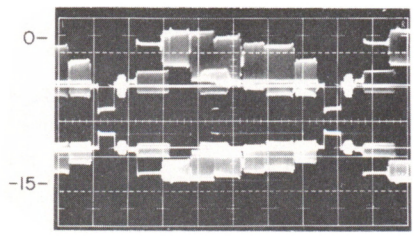
Video Input

The video input circuit (figure 96) provides control of the video gain in order to establish the video input signal at the desired level.

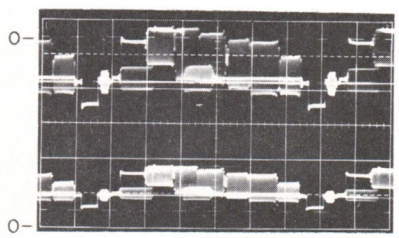




A. Top: Q1 base
Bottom: Q1 emitter
Both: 0.5 v/cm, 10 μs/cm



B. Top: Q1 emitter, 0.5 v/cm
Bottom: Q2 collector, 2 v/cm
Both: 10 μs/cm



C. Top: Q1 emitter, 0.5 v/cm
Bottom: Q4 collector, 5 v/cm
Both: 10 μs/cm

Figure 96—Video Amplifiers and Gain Control, Schematic Diagram and Typical Waveforms

Video from the CATC Video module or bypassed monochrome video is fed to the base of emitter follower Q1.

The video output of the emitter follower, Q1, is direct coupled to the base of Q2, the video gain control. In addition to Q2, the gain control circuit consists of a light-sensitive assembly comprising photo-cell V1 and two lamps DS1, DS2; the light control transistor, Q41, the video gain and level potentiometer, R87, and the associated local/remote control relay, K3.

Although K3 is wired for remote control operation, the LOCAL/REMOTE switch, (which is part of the Standards Switch) is wired for local operation only. Therefore the existing wiring on the LOCAL/REMOTE switch must be modified to accommodate remote operation. Until these modifications are made K3 cannot be energized, and the video gain varied only by operating the LOCAL VIDEO LEVEL potentiometer, R87. Instructions covering the wiring changes necessary for remote operation are given on the individual machine instruction book.

The video gain of Q2 is controlled by the resistance introduced into the emitter by the photo-cell. This, in turn, is determined by the setting of VIDEO LEVEL potentiometer, R87. Potentiometer R87 controls the amount of current flowing through the light control, Q41, and thus the intensity of illumination of the two lamps, DS1, DS2. The light from the two lamps is transmitted through a plexiglass prism to the photocell, which acts as a variable resistor. The resistance of the photocell is inversely proportional to the intensity of the light, i.e., as the light intensity increases the resistance of the photocell decreases and vice versa. Use of a light sensitive circuit makes possible dc control of the video level from a distant remote location. This type of circuit prevents video frequency losses that normally might be ex-

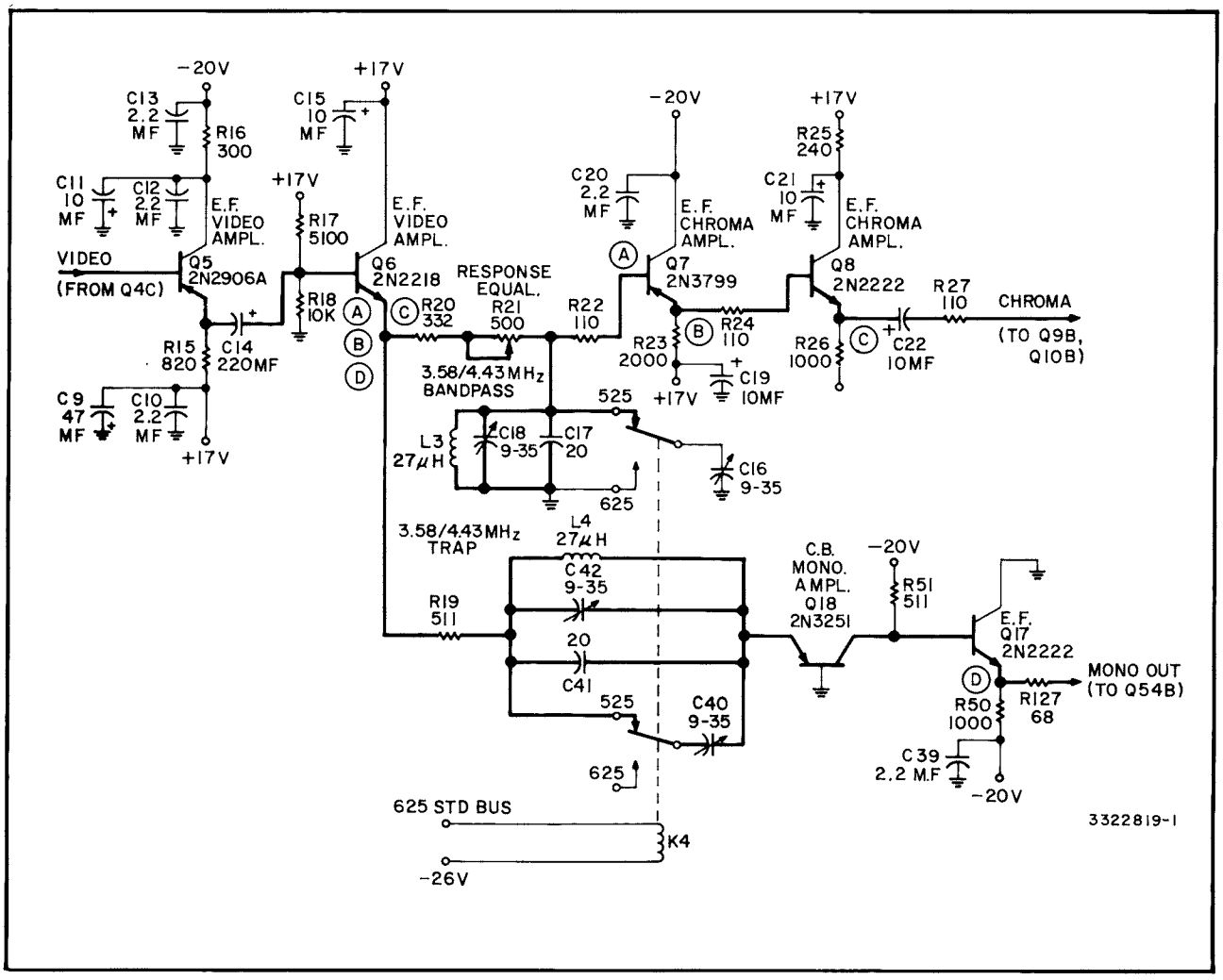
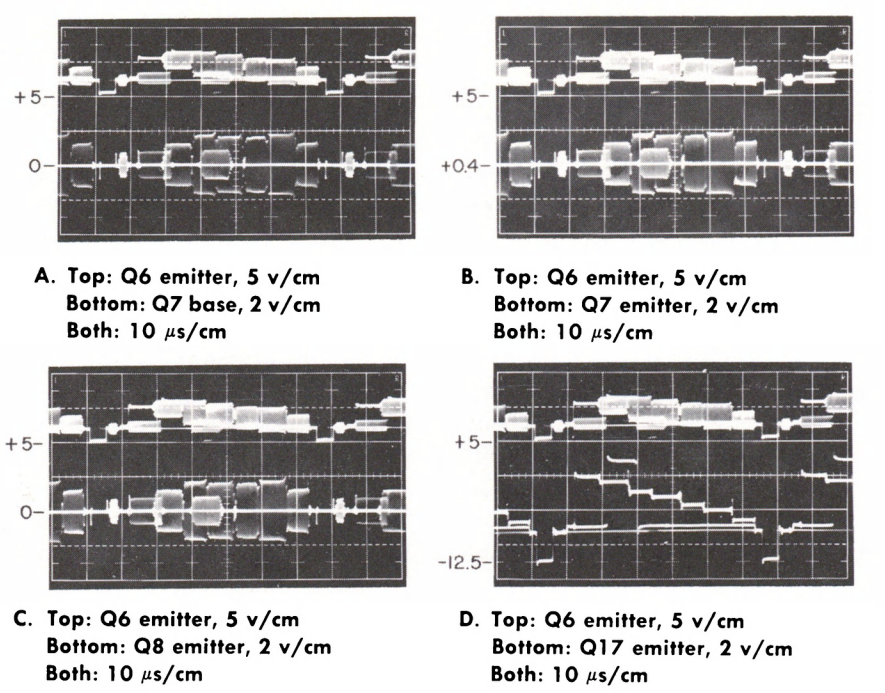


Figure 97—Monochrome and Chroma Signal Separation, Schematic Diagram and Typical Waveforms



A. Top: Q6 emitter, 5 v/cm
Bottom: Q7 base, 2 v/cm
Both: 10 μs/cm

B. Top: Q6 emitter, 5 v/cm
Bottom: Q7 emitter, 2 v/cm
Both: 10 μs/cm

C. Top: Q6 emitter, 5 v/cm
Bottom: Q8 emitter, 2 v/cm
Both: 10 μs/cm

D. Top: Q6 emitter, 5 v/cm
Bottom: Q17 emitter, 2 v/cm
Both: 10 μs/cm

Figure 97—Monochrome and Chroma Signal Separation, Schematic Diagram and Typical Waveforms (Continued)

pected if long lengths of cable were run directly from the emitter of Q2 to a video level control at some remote point.

The video output at the collector of Q2 is dc coupled across R12 to the base of Q4, the video amplifier. Coil L2 in the collector of Q2 provides high frequency compensation. The amplified video output at the collector of Q4 is direct coupled to the base of Q5, an emitter follower (figure 97). Transistor Q5 and the succeeding emitter follower, Q6, serve as the input to the two channel video circuit where monochrome and chroma are separated.

Monochrome and Chroma Separation

As shown in figure 97, the video output at the emitter of Q6 is fed simultaneously to two parallel resonant circuits. These two circuits are complementary in that one passes the chroma frequency components and the other rejects it. As a result, the monochrome and the chroma frequency components are separated. Each of these frequency components is then fed to a different circuit branch or channel for processing. Separate channels are necessary because the subsequent monochrome processing involves clamping, clipping, and new pedestal level. This would interfere with burst and other frequency elements of the chroma component which extend below the blanking level; therefore the monochrome and the chroma components are processed separately.

The video input to the chroma channel is dc coupled by R20, potentiometer R21, and R22 across a parallel resonant circuit to the base of Q7, an emitter follower chroma amplifier. Potentiometer R21, designated RESPONSE EQUALIZER, is an internal control sealed with a red compound to indicate the factory setting should not be disturbed. The parallel resonant circuit or tank consists of L3, variable capacitor C18, C17, and variable capacitor C16. Variable capacitor C16 is a switchable frequency determining component which establishes the subcarrier frequency at which the tank resonates, (i.e., 3.58 MHz on 525 lines or 4.43 MHz on 625 lines). Capacitor C16 is controlled by K4 in conjunction with the standards switch. When the 525-line standard is selected K4 is deenergized and C16 is switched into the tank circuit; when 625 line is selected K4 is energized and C16 is switched out of the tank circuit. Since the tank circuit is in parallel with the video signal, it provides maximum transfer of the resonant signal, while rejecting other frequencies outside the resonant frequency range. Thus only the chroma portion of the video signal is passed (figure 97A). Both variable capacitors (C16, C18) in the band-pass circuit are internal controls sealed with a red com-

pound; therefore the factory settings should not be disturbed.

The chroma signal at the emitter of Q7 (figure 97B) is dc coupled by R24 to the base of Q8, an emitter follower chroma amplifier. The cascaded emitter followers, Q7, Q8, reduce loading by the succeeding chroma clamp circuitry on the tank or subcarrier bandpass circuit. The chroma signal at the emitter of Q8 (figure 97C) is coupled by C22 and R27 to the bases of Q9, Q10, a C.S.E.F. in the Chroma clamp circuit.

The video input to the monochrome channel is fed through R19 and the parallel resonant circuit consisting of L4, variable capacitor C42, C41, and variable capacitor C40, to the emitter of Q18, a common base monochrome amplifier. This tank circuit is also resonant at the subcarrier frequency. But since it is in series with the signal, it offers maximum impedance to the subcarrier frequency and only the monochrome frequency component is passed. The monochrome tank circuit is similar to its chroma counterpart in that a switchable frequency determining component, variable capacitor C40, is used to resonate the tank at the subcarrier frequency appropriate to the line standards in use. Variable capacitor C40 is likewise controlled by K4 and the standards switch, and is switched into the chroma rejection circuit on 525-line standards and out of the circuit on 625-line standards. Both variable capacitors, C40, C42, are internal controls sealed with a red compound; therefore do not disturb the original factory adjustment.

The monochrome output at the collector of Q18 is fed to an emitter follower, Q17. The output at the emitter of Q17 (figure 97D) is dc coupled across R127 to another emitter follower, Q54. The two emitter followers isolate the chroma rejection circuit from the succeeding C.S.E.F. in the monochrome back porch clamp circuit.

Monochrome Back Porch Clamp

The clamp circuit, shown in figure 98, clamps the back porch of the monochrome signal to a dc reference potential.

The monochrome signal at the emitter of Q54 is dc coupled across R129 to the bases of Q55, Q56, the first of two C.S.E.F. (figure 98B). The monochrome output at the emitters of Q55, Q56 is fed

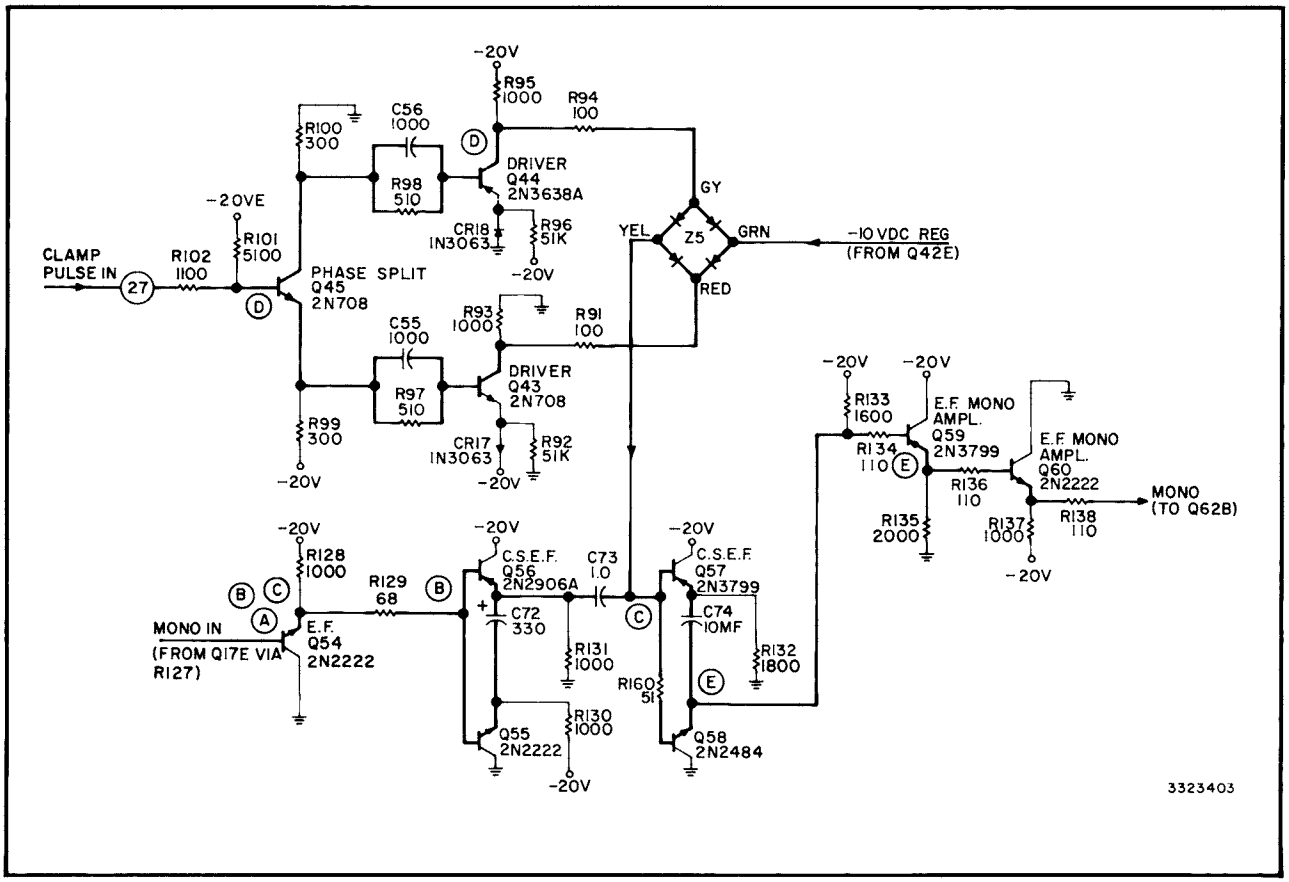
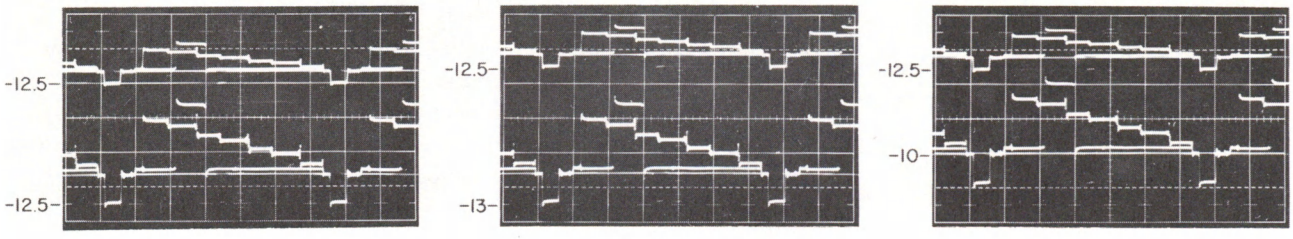


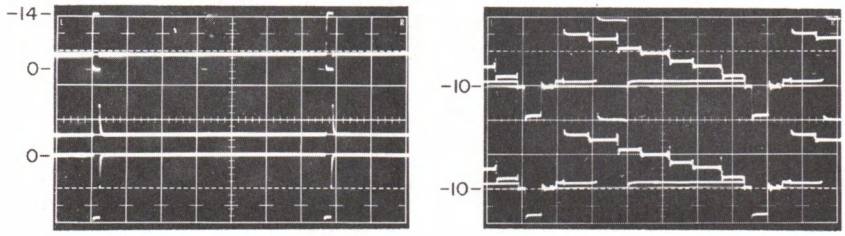
Figure 98—Monochrome Back Porch Clamp, Schematic Diagram and Typical Waveforms



A. Top: Q17 base, 5 v/cm
Bottom: Q54 base, 2 v/cm
Both: 10 μs/cm

B. Top: Q54 base, 5 v/cm
Bottom: Q55/Q56 base, 2 v/cm
Both: 10 μs/cm

C. Top: Q54 base, 5 v/cm
Bottom: Q57 base, 2 v/cm
Both: 10 μs/cm



D. Top: Q45 base, 5 v/cm
Middle: Q44 collector, 10 v/cm
Bottom: Q43 collector, 10 v/cm
All: 10 μs/cm

E. Top: Q58 emitter
Bottom: Q59 emitter
Both: 2 v/cm, 10 μs/cm

Figure 98—Monochrome Back Porch Clamp, Schematic Diagram and Typical Waveforms (Continued)

through the clamp coupling capacitor, C73, to the bases of the second C.S.E.F., Q57, Q58 (figure 98C). The two C.S.E.F. are non-saturating amplifiers, with the emitters of each following in phase the positive- and negative-going signal excursions. With a C.S.E.F. arrangement, the output obtained is, in effect, push-pull. Capacitor C72 serves as a dc blocking capacitor between the emitter of Q55 and Q56, thus preventing small differences in the dc potential between these two elements from upsetting the quiescent bias conditions. Likewise C74 in the emitter circuit of Q57 and Q58.

The −10 volt clamp potential is interposed in the monochrome signal at the output side of C73 by the clamp quad, Z5, during the back porch interval. The clamp quad, Q5 is turned on during this interval by keying pulses which are derived from the clamp pulse.

The clamp pulse originates in the Sync Logic module. It is a 10-volt positive-going pulse approximately 1.3 microseconds wide, whose leading edge is timed to the trailing edge of sync. The incoming clamp pulse is dc coupled across R102 to the base of Q45, a phase splitter (figure 98D). The phase splitter, Q45, normally cut off, is driven into conduction when the positive-going pulse is applied to its base. The resistance values in the collector and the emitter circuit of Q45 are the same; therefore the opposite polarity output pulses at each of these elements are of equal amplitude. The phase splitter output pulses, negative-going at the collector, positive-going at the emitter, are coupled through identical RC networks to the bases of the clamp quad drivers, Q44 and Q43, respectively. Capacitors C55 and C56 in the coupling networks improve or speed up the rise time of the loading edge of the pulses.

The collector of driver Q44 is connected at the junction of the anodes of the clamp quad (Z5) diodes and the collector of driver Q43 is connected to the junction of the cathodes. Since both drivers are normally cut off, the collector of Q44 is at −20 volts and the collector of Q43 is at zero or ground potential. Therefore the clamp quad, Z5, is reversed biased, hence cut off. The clamp quad driving pulses are timed to occur at the horizontal rate during the back porch interval. When the clamp drivers are driven into conduction by the phase splitter output pulses, the positive-going pulse at the collector of Q44 and the negative-going pulse at the collector of Q43 forward biases the clamp quad and the latter conducts. The −10 volt clamp potential is then passed through the low impedance of the conducting quad to the clamp capacitor C73, clamping the back porch of the monochrome signal being applied to C.S.E.F. Q57, Q58.

Following the C.S.E.F., Q57, Q58, are three emitter followers in cascade, Q59, Q60 and Q61. The clamped monochrome signal at the emitters of Q57,

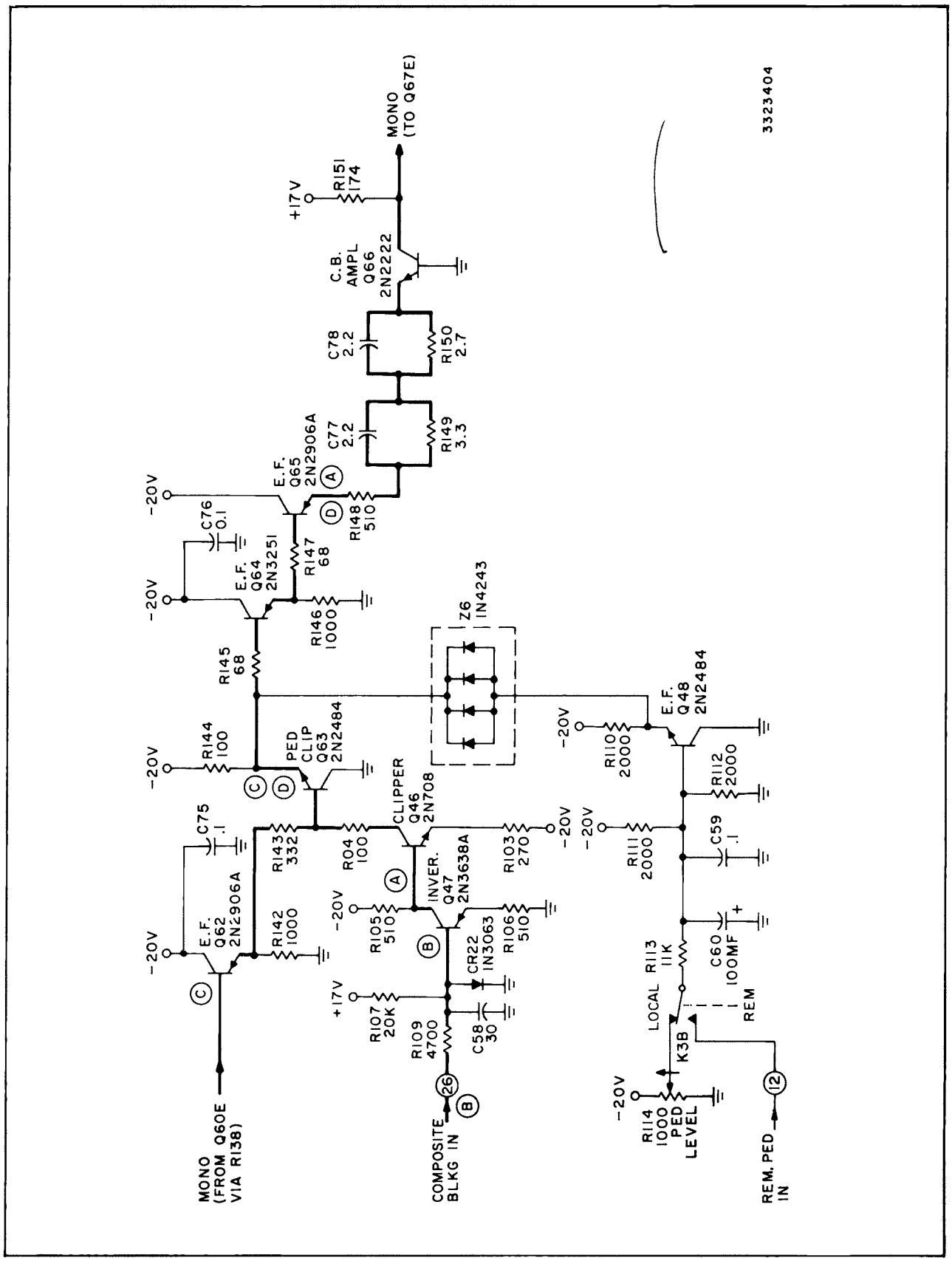
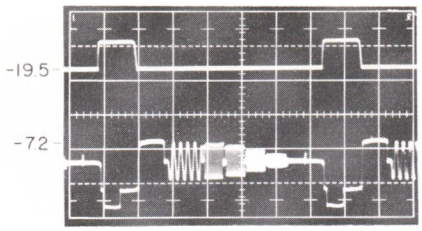
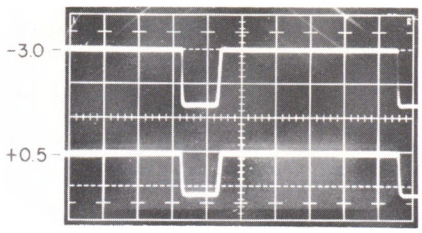


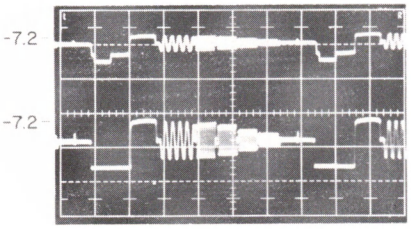
Figure 99—Pedestal Level, Schematic Diagram and Typical Waveforms



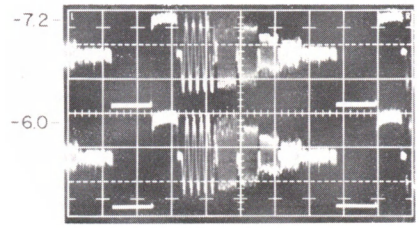
A. Top: Q47 collector, 5 v/cm
Bottom: Q62 base, 2 v/cm
Both: 10 μs/cm



B. Top: P1 pin 26
Bottom: Q47 base
Both: 10 μs/cm



C. Top: Q62 base, 5 v/cm
Bottom: Q63 emitter, 2 v/cm
Both: 10 μs/cm



D. Top: Q63 emitter
Bottom: Q65 emitter
Both: 1 v/cm, 10 μs/cm
PLAY mode

Figure 99—Pedestal Level, Schematic Diagram and Typical Waveforms (Continued)

Q58 (figure 98E) is dc coupled through all three amplifiers. The cascaded arrangement provides isolation and a low impedance source for driving the succeeding circuits. The clamped monochrome signal is taken from this stage. This is the emitter of Q60 at the junction of R138 and R139. From here the signal is fed to Q62, an emitter follower in the blanking adder and pedestal clipper circuit.

Blanking Adder, Pedestal Clipper and New Pedestal Insertion

The blanking adder and pedestal clipper circuit (figure 99) eliminates sync and blanking from the input signal, and provides a new and an adjustable pedestal level for the monochrome signal.

The incoming clamped monochrome signal is fed to the base of Q62, an emitter follower (figure 99C). At the same time, composite blanking, which originates in the Sync Logic module, is dc coupled across R109 to the base of Q47, an inverter (figure 99B). The inverter, Q47, and the succeeding direct coupled amplifier, Q46, are normally cut off. The inverter, Q47, is cut off due to the reverse bias on its base which is developed across the network consisting of R107 and CR22 connected between +17 volts and ground. In this state, the collector of Q47 is at −20 volts, and since the base of Q46 is returned directly to the collector of Q47, the −20 volts reverse biases the base of Q46, cutting off the latter.

The incoming blanking signal applied to the base of Q47 is a 5-volt negative-going pulse. This drives Q47 into conduction and the collector potential rises from −20 volts (figure 99A). The positive-going pulse at the collector of Q47 is fed to the base of Q46 causing the latter to conduct. The negative-going blanking pulse at the collector of Q46 is fed to the base of Q63 the pedestal clipper.

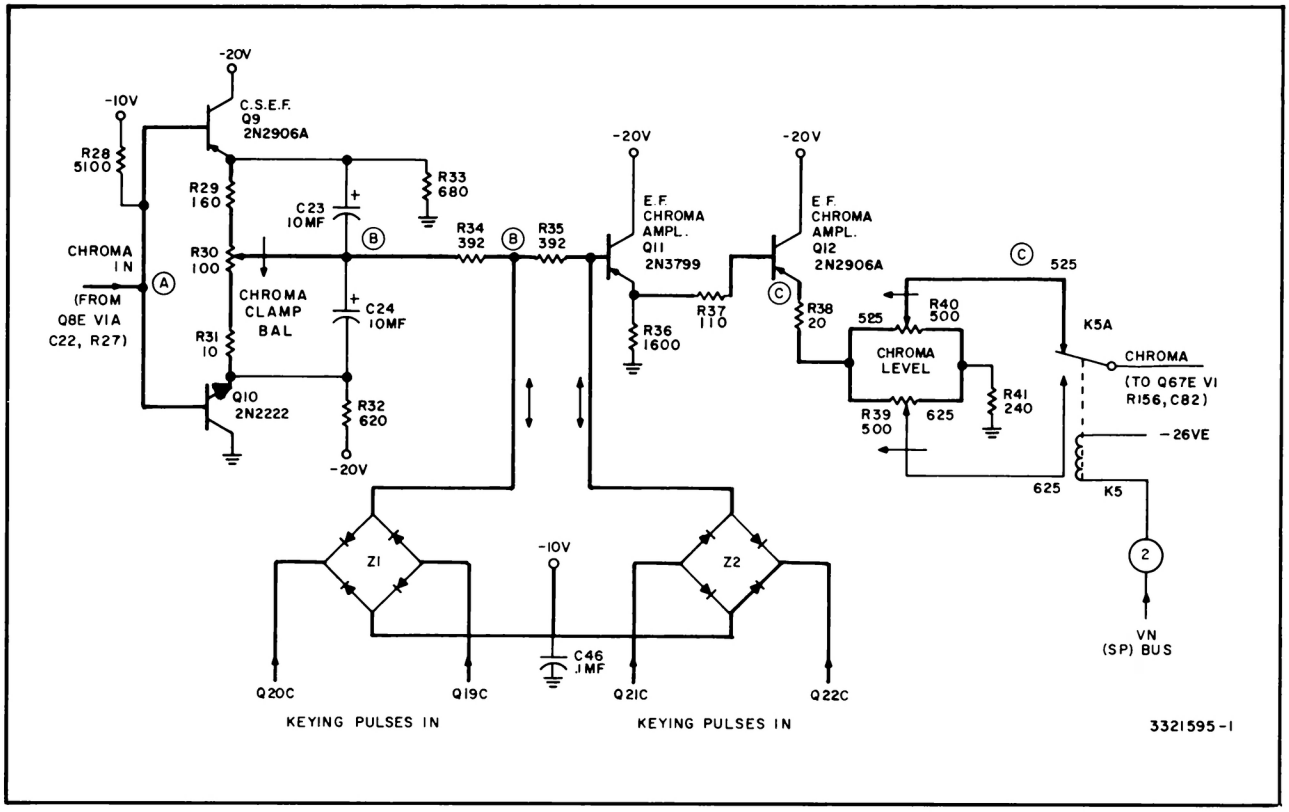
The emitter of Q62 and the collector of Q46 form a common connection at the junction of R143, R104, and the base of Q63, the pedestal clipper driver. Thus at the base of Q63, the negative-going pulse output of Q46 is added to the existing blanking component in the monochrome output of Q62 (figure 99C). As a result, the blanking component of the monochrome signal, which was formerly approximately 0.3 volt (−9.7 volts to −10 volts), is now 4 volts (−9 volts to −13 volts). Increasing the amplitude of blanking in this manner insures that noise or switching transients present in the original blanking and sync portion of the signal will be eliminated by the clipper, Z6.

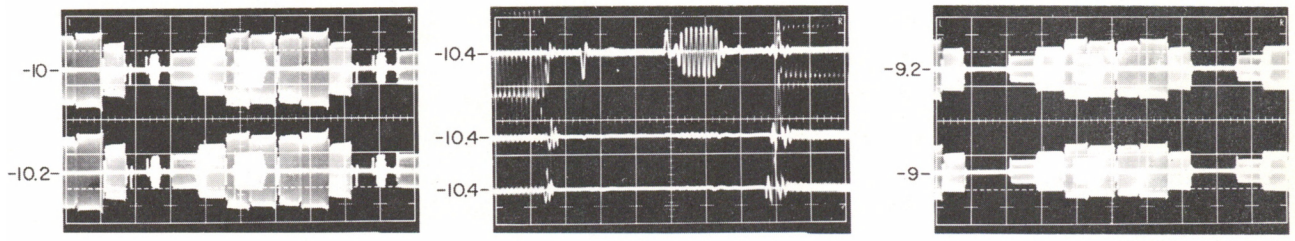
The monochrome output at the emitter of Q63, the pedestal clipper driver is fed across the clipper,

Z6. The clipper is comprised of four diodes connected in parallel. This array minimizes the individual diode impedance when the clipper is conducting. The clipping threshold is approximately −10 volts. Therefore that portion of blanking below the −10 volt level is eliminated by the clipper (figure 99D).

The level at which clipping takes place establishes the new pedestal level. The clipping or new pedestal level is determined by a dc control voltage applied to the anodes of the clipper diodes, via the control transistor, Q48, an emitter follower. Local or remote control of the pedestal level is provided by K3B. When local control is employed, the pedestal level is established by potentiometer, R114, the PED LEVEL. The PED LEVEL control permits the pedestal level to be varied from 0 to 20 IRE units.

The monochrome signal now with a new pedestal level and the old blanking and sync removed is fed through two dc coupled emitter followers, Q64 and Q65 (figure 99D). From the emitter of Q65, the monochrome signal is coupled by two RC networks to a common base amplifier, Q66. The RC networks, in effect, improve the middle and high frequency end of the band by attenuating the low frequency





A. Top: Q9/Q10 base
Bottom: Junction C23, C24
Both: 2 v/cm, 10 μs/cm

B. Top: Junction C23, C24, 1 v/cm
Middle: Junction R34, R35, 0.5 v/cm
Bottom: Q11 base, 0.5 v/cm
All: 2 μs/cm

C. Top: Q12 emitter
Bottom: Arm R40
Both: 2 v/cm, 10 μs/cm

Waveforms in PLAY mode.

Figure 100—Chroma Control, Schematic Diagram and Typical Waveforms

end. The monochrome output at the collector of Q66 is fed to Q67, another common base amplifier, which serves as the video combiner stage.

Clamped Chroma and Chroma Level

To return to the chroma frequency processing. As previously described, a band-pass filter resonant at the subcarrier frequency eliminates all but the chroma information from the video signal. The remaining chroma frequency components are then coupled through two isolation emitter followers to the chroma clamp and chroma level circuit, as shown in figure 100.

The chroma clamp eliminates input burst during color tape playback by clamping the entire blanking interval at approximately −10.5 volts. Regenerated burst is inserted later, when the chroma and the monochrome frequency components are re-combined. The chroma level control enables the amplitude of the clamped chroma signal to be varied so that it equals that of the monochrome signal, when the two signals are subsequently re-combined.

In the E-E mode the regenerated burst circuit in the Color Processor module is disabled, therefore regenerated burst is not available for subsequent insertion in the chroma signal. In the absence of regenerated burst, it is necessary to permit input burst to pass. To do this the clamp pulse is interrupted for approximately 4 microseconds by a blanking notch pulse. This discontinuity takes place during the period in the blanking interval that burst would normally be present, thus the existing input burst is allowed to pass. (A more detailed analysis of the blanking notch pulse and its function is given later, in the discussion of the Chroma Clamp and Blanking Notch Circuit.)

The chroma signal at the emitters of the C.S.E.F., Q9, Q10 (figure 100A) is taken across the CHROMA CLAMP BAL potentiometer, R30, and is fed via R34 and R35 across the two cascaded clamp quads, Z1 and Z2 to the base of Q11, an emitter follower. The CHROMA CLAMP BAL potentiometer, R30, is adjusted to equalize the output impedance across the emitters of Q9, Q10. This is an internal control and normally does not require re-adjustment.

The clamp quads, Z1 and Z2, are keyed on during the horizontal blanking interval. When the quads conduct, the clamp potential is passed by the low impedance of clamp diodes, clamping the entire blanking interval at approximately −10.4 volts (figure 100B). At the same time, input burst is fed to ac ground through C46. The purpose of cascade clamping is to obtain the attenuation required to eliminate virtually all of the original input burst. The clamped chroma signal is fed through two dc coupled isolation emitter followers, Q11 and Q12.

The clamped chroma output at the emitter of Q12 (figure 100C) is taken across either of two CHROMA LEVEL potentiometers, R40 (525-line standards) or R39 (625-line standards). The potentiometer the output is taken across is determined by the line standards selector, relay K5A. When K5 is deenergized its contacts are closed to the 525-line standard CHROMA LEVEL potentiometer, R40. When 625-line standards is chosen, K5 is energized by a control signal (ground) from the VN (special) bus, and the chroma output is selected across the 625-line standard CHROMA LEVEL potentiometer, R39. In either case, the clamped chroma signal is then fed via R156 and C82 to the emitter of Q67. The latter, a common base amplifier, serves as the video combiner where monochrome and chroma are re-combined and re-generated burst is inserted. The CHROMA LEVEL potentiometers are internal controls. Both are sealed with a red compound, indicating a factory adjustment which should not be disturbed in the field.

Chroma Clamp and Blanking Notch

During playback of color tape, the clamp circuit (figure 101) interposes a clamp reference in the chroma signal blanking interval which clamps the entire blanking interval at approximately −10.4 volts, thus eliminating input burst. Later, when the chroma and monochrome components are again combined, regenerated burst, which originates in the Burst Processor module, is inserted in the blanking interval. The −10 volt clamp potential is passed by a pair of diode quads, Z1 and Z2, in cascade. Double clamping insures that practically all vestiges of input burst are eliminated during the horizontal blanking interval. The clamp quads are controlled by keying pulses developed from horizontal blanking pulses.

The blanking notch circuit is active only in the E-E mode when burst is present. The purpose of this circuit is to enable input burst to pass, since, in the E-E mode, regenerated burst is not available for reinsertion in the chroma signal. For the present it is sufficient to state the ultimate effect of this circuit which is to unclamp the blanking interval during the period normally occupied by burst, thus permitting input burst to pass.

As shown in figure 101, composite blanking, which originates in the Sync Logic module is coupled across

R71 to the base of Q24, an inverter. Capacitor C45 in parallel with R71 helps prevent the pulse edges from rounding off by speeding up the pulse rise time. The inverter, Q24, is normally cut off by the reverse bias applied to its base across the voltage divider consisting of R70, R71 and R72 connected from +20 volts to ground. The incoming negative-going blanking pulse overcomes the reverse bias on the base and Q24 is driven into conduction. At this point, assuming color tape playback, no useable signal is applied to the emitter of Q24 from emitter follower Q51 in the blanking notch generator circuit. During playback, the output of the blanking notch generator circuit is disabled. When Q24 conducts, a 5-volt positive-going pulse appears at the collector and is direct coupled to Q23, a phase inverter.

The phase splitter, Q23, is cut off during the interval between blanking pulses since the base is returned to −20 volts at the collector of Q24. Transistor Q23 is driven into conduction when the 5-volt positive-going pulse is applied to its base from the collector of Q24. The complementary output of the phase splitter is a 5-volt negative-going pulse at the collector and a 5-volt positive-going pulse at the emitter (figure 101E, F). These pulses are applied in phase opposition to the bases of Q21, Q22, the driver pair for clamp quad Z2, and to the bases of Q19, Q20, the driver pair for clamp quad Z1.

The TILT potentiometer, R67, in the collector of Q23 is adjusted to compensate for differences in the transistor parameters between quad Z1 driver Q19 and quad Z2 driver Q21. In effect, it insures that the opposite polarity gating pulse output of each quad driver pair will be of equal amplitude. The TILT potentiometer, R67, is an internal control sealed with a red compound. This indicates it is a factory adjustment which should not be disturbed in the field. The TRANSIENT SUPPRESSOR, variable capacitor C43, an internal control in the emitter of Q23, functions primarily in the E-E mode. The TRANSIENT SUPPRESSOR is adjusted to eliminate any sharp switching spikes during the blanking notch pulse period. Ordinarily this control requires no further adjustment.

Since both clamping circuits are identical only one, clamp quad Z2 and its associated drivers Q21 and Q22 will be described. Normally both drivers are cut off; the collector of Q21 is at −20 volts and the collector of Q22 is at ground. Thus the clamp quad, Z2, is also cut off since the quad diodes are reverse biased, with the anodes returned to −20 volts at the collector of Q21 and the cathodes returned to ground at the collector of Q22. When the complementary pulse output of phase splitter Q23 is applied to the bases of Q21 and Q22 both transistors are driven into conduction. The collector of Q21 rises from −20 volts to −10 volts and the collector of Q22 drops from ground to −10 volts (figure 101B). The positive- and negative-going gating pulses appearing at the collectors of Q21 and Q22 forward bias quad Z2 and the latter conducts, passing the −10 volt clamp potential.

As mentioned earlier, Z1 and Z2 are connected in cascade since double clamping is needed to completely suppress input burst. During horizontal blanking both quads conduct together, and the −10 volt clamp is interposed in the path of the chroma signal at two successive points, as was shown in figure 101B.

To return to the blanking notch generator circuit figure 101). In the E-E mode, the regenerated burst output circuit in the module is disabled; therefore in the absence of regenerated burst, input burst must be allowed to pass. However, since the clamp quads are still keyed on at a horizontal rate regardless of the mode, E-E or PLAY, the entire blanking interval continues to be clamped. This means that if input burst is to pass, the clamp quad keying pulses, hence the clamp potential, will have to be discontinued during that period of time in the blanking interval that input burst is normally present. Therefore a narrow blanking notch pulse, derived from the trailing edge of Gated Horizontal, is inserted in the horizontal blanking pulse. The timing of the blanking notch pulse is such that it interrupts the horizontal blanking pulse during the period burst is normally present. The conduction period of the clamp quads depends upon the duration of the quad keying pulses which are derived from horizontal blanking. Therefore any discontinuity or interruption in the duration of the horizontal blanking pulses means the clamp quads will be turned off for the time the discontinuity exists. Thus during the time the blanking notch pulse is present, the clamp quads are cut off and input burst is allowed to pass.

The timing of the blanking notch pulse with respect to burst is shown in figure 102. Burst normally follows the trailing edge of sync by 0.5 microsecond; therefore, the blanking notch pulse produced by a boxcar pulse derived from the trailing edge of gated horizontal is timed to occur during the input burst interval.

A more detailed analysis as to how the blanking notch pulse circuit functions is given below.

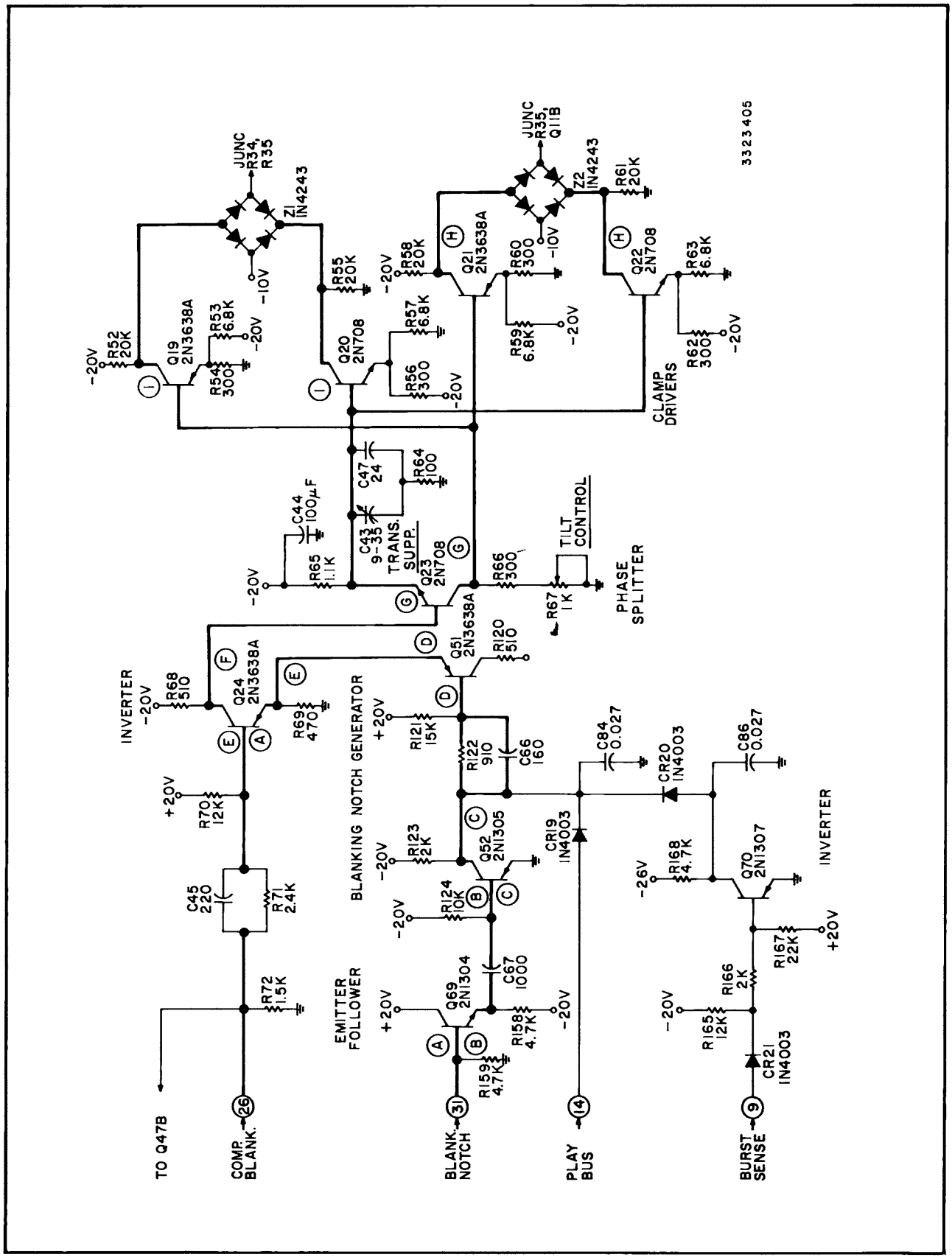
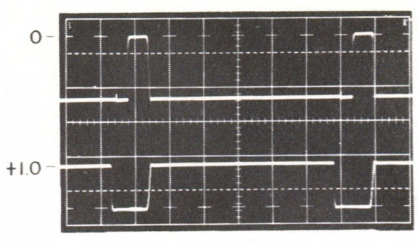
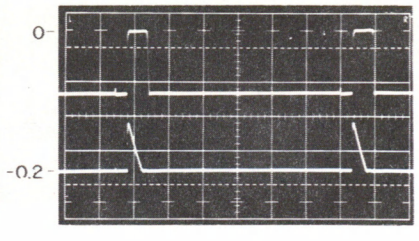


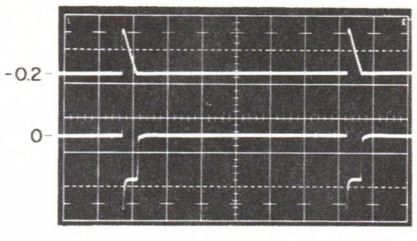
Figure 101—Clamp Key Pulse, Schematic Diagram and Typical Waveforms



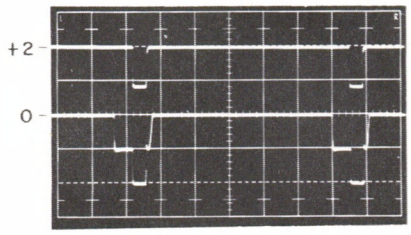
A. Top: Q69 base
Bottom: Q24 base
Both: 5v/cm, 10 μs/cm
E-E



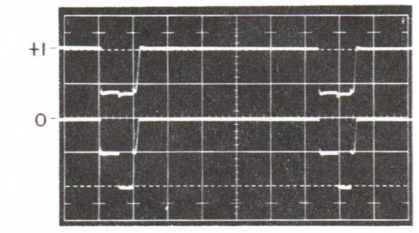
B. Top: Q69 base
Bottom: Q52 base
Both: 5v/cm, 10 μs/cm
E-E



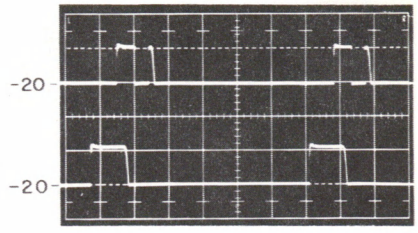
C. Top: Q52 base, 5 v/cm
Bottom: Q52 collector, 0.5 v/cm
Both: 10 μs/cm (E-E)



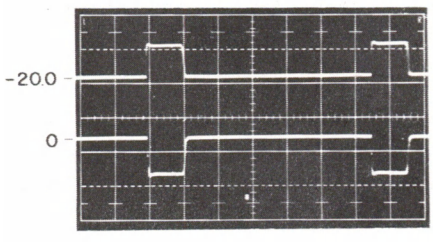
D. Top: Q51 base, 10 v/cm
Bottom: Q51 emitter, 5 v/cm
Both: 10 μs/cm (E-E)
Color signal on Video Input



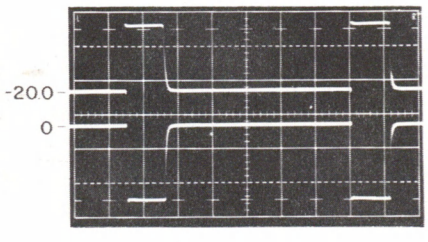
E. Top: Q24 base, 5 v/cm
Bottom: Q24 emitter, 5 v/cm
Both: 10 μs/cm (E-E)
Color signal on Video Input



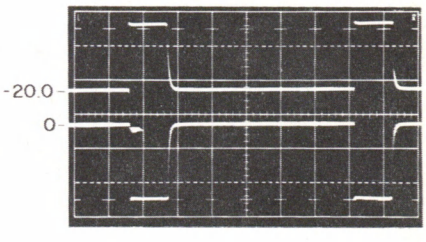
F. Top: Q24 collector (E-E)
Bottom: Q24 collector (PLAY)
Both: 5v/cm, 10 μs/cm
Color signal on Video Input



G. Top: Q23 emitter
Bottom: Q23 collector
Both: 5v/cm, 10 μs/cm
PLAY mode



H. Top: Q21 collector
Bottom: Q22 collector
Both: 5v/cm, 10 μs/cm
PLAY mode



I. Top: Q19 collector
Bottom: Q20 collector
Both: 5v/cm, 10 μs/cm
PLAY mode

Figure 101—Clamp Key Pulse, Schematic Diagram and Typical Waveforms (Continued)

The Blanking Notch pulse which originates in the Color Proc module is fed via pin P1-31 to the base of Q69, an emitter follower (figure 101A). The incoming signal is a positive going pulse. From the emitter of Q69, the pulse is coupled across a differentiator consisting of C67 and R124 to the base of a boxcar, Q52.

The boxcar, Q52, is normally saturated and the collector is at ground potential. The positive-going spike of the differentiated pulse charges C67 to approximately +7 volts (figure 101B). The positive-going spike on the base of Q52 drives the latter to cutoff and the collector potential falls to approximately −13 volts. With Q52 cut off, C67 begins to discharge toward −20 volts from approximately +7 volts. When the voltage across C67 becomes just slightly negative with respect to ground, Q52 is again driven into conduction and the collector potential rises to ground. As a result the output at the collector of Q52 is a 13 volt negative-going pulse, approximately 4 microsecond wide (figure 101C). This is the blanking notch pulse and it is coupled across R122 to the base of Q51, an emitter follower.

Transistor Q51 is normally biased at cutoff by approximately +1 volt on the base. This positive potential is developed across the divider formed by R121 and R122 connected from +20 to ground at the collector of Q52. Capacitor C66 in parallel with R122 serves as a speedup capacitor to preserve the fast rise time of the negative-going leading edge of the blanking notch pulse. The blanking notch pulse drives Q51 into conduction (figure 101D), and the output pulse appearing at the emitter is direct coupled to the emitter of Q24, the inverter to which incoming blanking is applied.

The inverter, Q24, normally cutoff, is driven into conduction when the incoming blanking is applied to its base. Once conducting, Q24 would continue to conduct until the end of the blanking pulse period. However, the blanking notch pulse, which is produced in this interim by the trailing edge of regenerated sync, appears at the emitter of Q24 (figure 101E). Since the notch pulse is negative with respect to the emitter of Q24, the latter is driven into cutoff and remains cutoff for the duration of the notch pulse, or approximately 4 microseconds. At the end of this time, Q24 resumes conduction, continuing for the remainder of the blanking pulse period (figure 101F). The result of this interruption is reflected as a discontinuity in the width of the output pulse at the collector of Q24. Thus the out of phase pulses appearing at the emitter and collector of Q23 have a serration or notch approximately 4 microseconds wide (figures 101E, F).

From here on the action of the rest of the circuit in producing the notched gating pulses for the clamp quads, Z1 and Z2, is the same as with the regular gating pulses. The discontinuity in the width of the gating pulses (figures 101H, I) now being applied across the clamp quads will cut them off for approximately 4 microseconds. During this time, the blanking interval goes unclamped enabling input burst to pass. At the end of the notch period, the gating pulse period resumes, and the remaining portion of the blanking interval is again clamped.

To prevent the blanking notch pulses from being interposed in the quad gating pulse during playback of color tape, the blanking notch circuit is disabled. During the interval between regenerated sync pulses, Q52 is saturated and the collector is at ground potential. At the same time Q51 is cutoff. With the arrival of sync, Q52 normally would go to cutoff deriving the notch pulse which would then be passed by Q51. However in the PLAY mode, the Play bus is at ground potential. Therefore as soon as the collector of Q52 goes slightly negative with respect to ground (figure 101C), CR19 becomes forward biased and ground potential is applied to the junction of R122 and the collector of Q52. Thus the notch pulse at the collector of Q52 is eliminated. The emitter of Q51 and the emitter of Q24 are tied together, forming a common connection. As long as the collector of Q52 is at ground potential, Q51 will remain cutoff since the potential on the emitter of Q51 will always be negative with respect to that on the base. Thus the pulse output at the collector of Q24 will be devoid of the notch pulse (figure 101F).

In addition, to prevent the notch pulse circuit from operating in the E-E mode for monochrome signals, the Burst Sense bus is inverted and applied to the same point. The inverted Burst Sense at the collector of Q70 becomes ground when burst is absent from the E-E signal. Thus, a good clean blanked back porch is preserved when there is no burst to be gated through.

Combined Video Output

The purpose of the video combiner and the video output circuit is (a) to combine the chroma and the monochrome components previously processed separately; (b) in PLAY mode, insert regenerated burst; and (c) to provide a low impedance output source for driving the video line to the Video Output module.

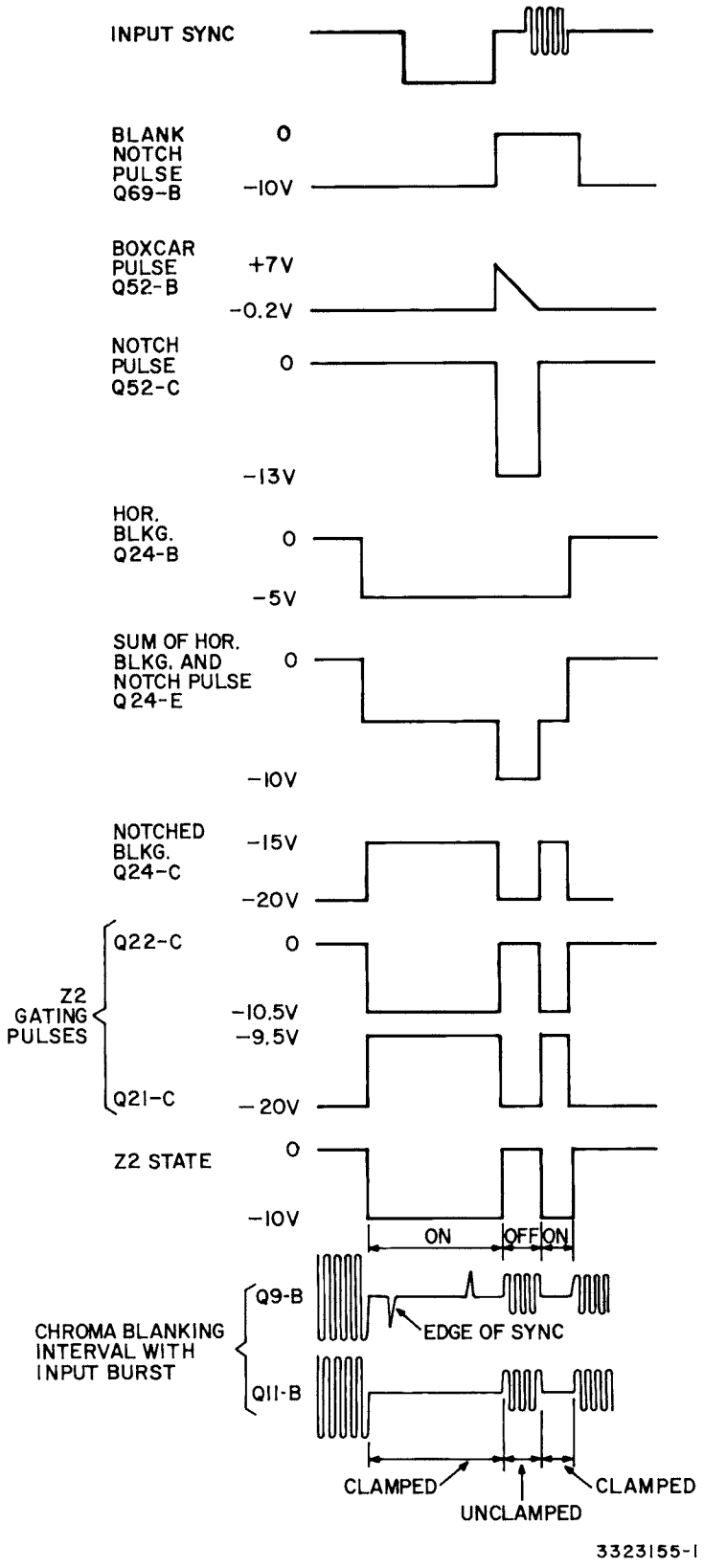
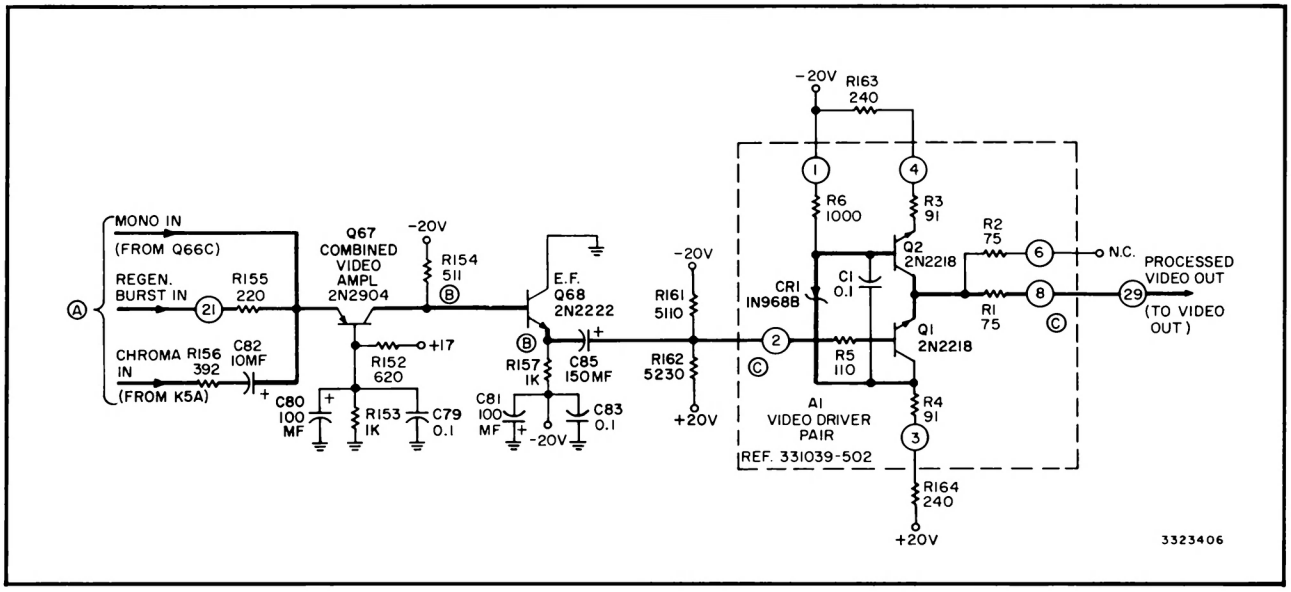


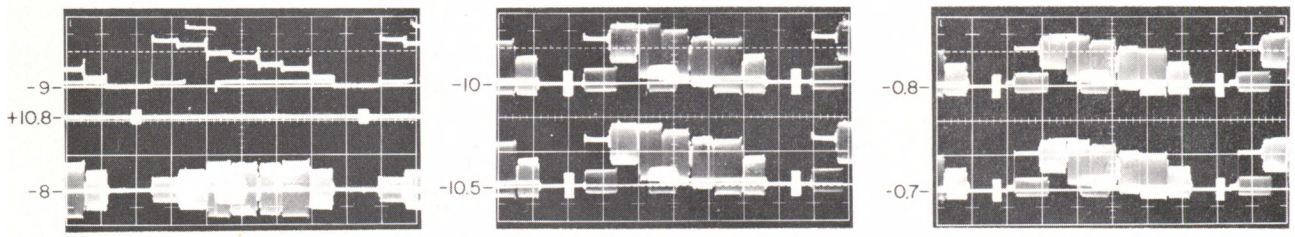
Figure 102—Development of Blanking Notch Pulse in E-E Mode

The video components being applied to this circuit have now been stabilized. The monochrome component was clamped, the old blanking removed, and new pedestal inserted. The chroma component was clamped, eliminating the original input burst along with any switching spikes or transients that might have occurred during the blanking interval. And clean new burst, regenerated in the Color Processor module, is now available.

As shown in figure 103, the three signals (figure 103A) are applied to the emitter of a common base amplifier, Q67, which serves as the signal combining stage. The combined video signal at the collector of Q67 is coupled through an isolation emitter follower, Q68 (figure 103B), to the base of the input transistor of a video driver pair. The latter consists of two transistors and associated circuitry, mounted on a sub-module designated A1.

The configuration of the video driver pair is such that A1-Q1 assumes the characteristics of both an emitter follower and a common emitter amplifier, while A1Q2 assumes those of a common emitter amplifier. The video input signal is applied across A1-R1 to the base of A1-Q1. The inverted output at the collector of A1-Q1 is coupled through the low impedance of Zener diode A1-CR1 and bypass capacitor A1-C1 to the base of A1-Q2. Although A1-CR1 presents negligible impedance to the signal current, losses occur at the higher video frequencies due to stray capacitance and other factors. Use of the bypass capacitor, A1-C1, helps to overcome such losses. Zener diode A-CR1 maintains a constant 20-volt difference between the collector of A1-Q1 and the base of A1-Q2. The output signal on the collector of A1-Q2, having been inverted also, is in phase with the signal on the emitter of A1-Q1. Since amplifier output video is taken at the emitter-collector junction





A. Top: Q65 emitter
Middle: P1-21
Bottom: Junction K5A, R156
Both: 2 v/cm, 10 μs/cm

B. Top: Q67 collector
Bottom: Q68 emitter
Both: 2 v/cm, 10 μs/cm

C. Top: A1-2, 2 v/cm
Bottom: A1-8, 1 v/cm
Both: 10 μs/cm

All waveforms in PLAY mode.

Figure 103—Video Combiner and Output Driver, Schematic Diagram and Typical Waveforms

of these two transistors, it contains components of the signal at each of these elements. This, in effect, is the same as push-pull output. The series amplifier arrangement of the video driver pair provides low source impedance for driving the video output line. The video output is fed through a 75-ohm resistor, A1-R1, to pin A1-8 (figure 103C). From the latter the signal is fed via pin P1-29 to the Video Output module.

Voltage Regulators

Virtually all of the dc operating voltages used throughout the Video Processor module are regulated. There are seven regulator circuits, five +20 volt (Q13, Q15, Q49, Q50, Q53), one −10 volt (Q42), and one +17 volt (Q16). See Video Processor schematic in the *Diagrams Manual*. The −20 volt regulators are similar to those used in the Video Output module; the −10 volt and +17 volt regulators are similar to those used in MATC Video module.

ADJUSTMENTS

CAUTION: Some internal variable reactance and resistance components are sealed with a red compound. This indicates that it is a factory adjustment which should not be readjusted in the field. If service is required, notify the RCA field representative.

The first two controls covered in the procedure below are external front panel controls. These are the VIDEO LEVEL (R87) and the PED (R114). The settings given for these controls represent the generally accepted nominal value of these signals. Individual station requirements may dictate some variation in these signal levels.

The remaining two controls, Transient Suppressor (C43), and the Chroma Clamp Balance (R30) are internal controls. These two controls have been adjusted at the factory, and their settings should not be disturbed in the course of normal operation or routine maintenance. However, should component replacement or some other reason necessitate readjustment, refer to the procedure, appropriate to the control requiring adjustment, below.

Video Level

1. Play back a color tape.

2. Press the OUT pushbutton on the CRO switcher and select the line (HOR) rate for display on the CRO.

3. Adjust the VIDEO LEVEL control for 100 units on the IRE scale.

Pedestal Level

1. Play back a color tape.

2. Press the OUT pushbutton on the CRO switcher and select the line (HOR) rate for display on the CRO.

3. Adjust the PED control for 7.5 units on the IRE scale.

Transient Suppressor Capacitor

1. Mount the Video Processor module in an extender and insert it in the machine.

2. Place the machine in the E-E mode of operation. Apply a monoscope signal or other monochrome signal without burst to the input of the machine.

3. Press the OUT pushbutton on the CRO switcher. Set the sweep of the CRO at the horizontal rate.

4. Observe the signal on the CRO; note that portion of the back porch normally occupied by burst. Adjust the Transient Suppressor capacitor, C43, for minimum transients at that point in the blanking signal where burst normally begins and at that point where burst normally ends.

5. Remove the extender and replace the Video Processor module in the machine.

Chroma Clamp Balance Potentiometer

1. Mount the Video Processor module in an extender and insert it in the machine.

2. Place the machine in the E-E mode of operation. Apply a monoscope signal or other monochrome signal without burst to the input of the machine.

3. Press the OUT pushbutton on the CRO switcher. Set the sweep of the CRO at the horizontal rate.

4. Observe the signal on the CRO; note that portion of the back porch normally occupied by burst. Adjust the CHROMA CLAMP BALANCE potentiometer, R30, so that the base line of that portion of blanking normally occupied by burst is a straight line. That is, no departure in blanking level in the form of a positive-going or negative-going notch appearing in the blanking area normally occupied by burst.

5. Remove the extender and replace the Video Processor module in the machine.

VIDEO OUTPUT MODULE

CIRCUIT DESCRIPTION

General

The video output module, shown on block diagram figure 104, combines the processed video from the Video Processor module and the regenerated sync from the Sync Logic module to form a composite video signal which is available at five separate outputs. A 0.5 microsecond delay line is inserted in the video path to equalize the propagation delay introduced by the sync signal path. High frequency roll-off is compensated for by the chroma circuits at the output of the delay line.

Sync gain control transistor Q5 is controlled locally by the SYNC LEVEL control located on the front panel of the module. If remote operation is used, a similar control on the remote panel is selected by relay K1.

Four −20 volt regulators are used to supply the video line driver circuits, sync adder circuits, and other circuits with a constant potential source under varying current conditions.

Video Delay and Chroma Control

As shown in the simplified schematic, figure 105, the processed video from the Video Processor module at P1-17 is fed to the 0.5 microsecond delay line, DL1. Figure 105A and B shows the waveforms at the input and output of the delay line. The delay line is a multi-section pi-type, encapsulated inductor-capacitor, fixed delay circuit whose output is terminated with a 75 ohm network to match the output impedance of the Video Processor module. The delay line compensates for the delay encountered by the sync signal while being operated upon in the sync separator and sync regeneration circuits. The delay ensures that the proper timing relationship is maintained between the video and regenerated sync when the latter is reinserted into the composite signal later.

Video through the delay line DL1 is applied to the base of Q13 via divider resistors R61, R2 and through resistor R63. One half of the delay line output amplitude is effectively fed to the base of Q13. One output from the emitter of Q13 (figure 105B) is coupled through the low frequency trimmer capacitor C41 and resistor R66, while another output is fed through a high frequency compensation network to the emitter of Q15.

High frequency gain can be varied by the network of trimmer potentiometer R69, CHROMA control potentiometer R27 and capacitors C51 and C53. This provides a frequency response that is essentially linear with frequency that can be varied from increasing gain with respect to frequency, through a flat response, to a decreasing gain with respect to frequency as illustrated on figure 106. Variable capacitor C41, used for low frequency compensation, and variable inductor L4, used for high frequency compensation, are both used to provide a flat frequency response.

Since the output of the module is approximately one volt of video, the input to the video line drivers should be approximately two volts. Taking into ac-

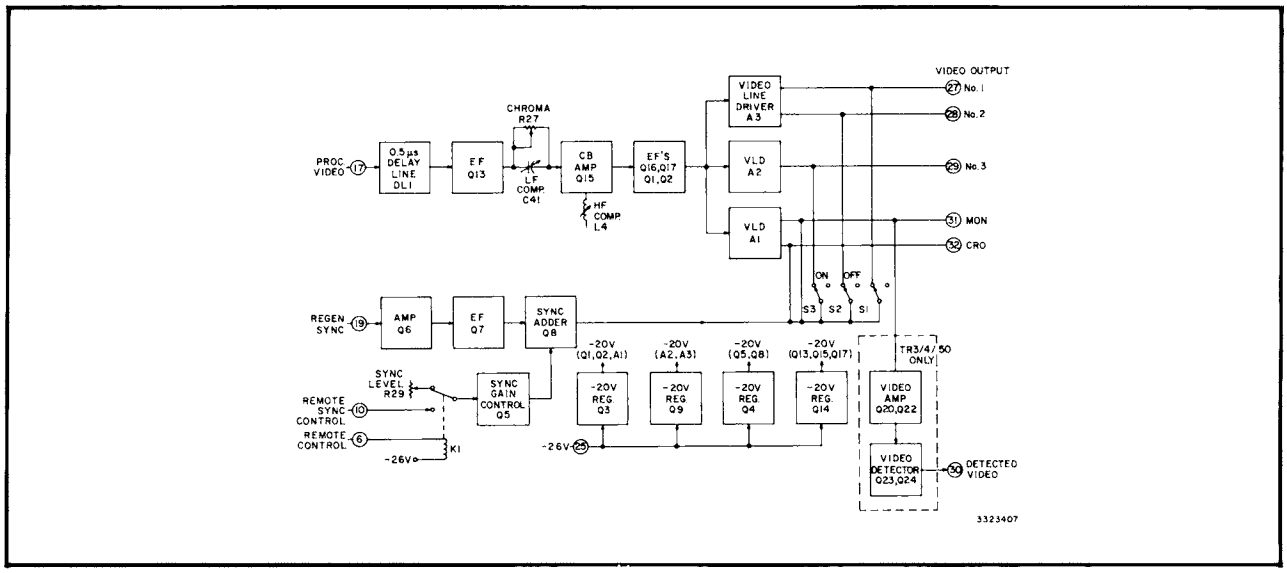
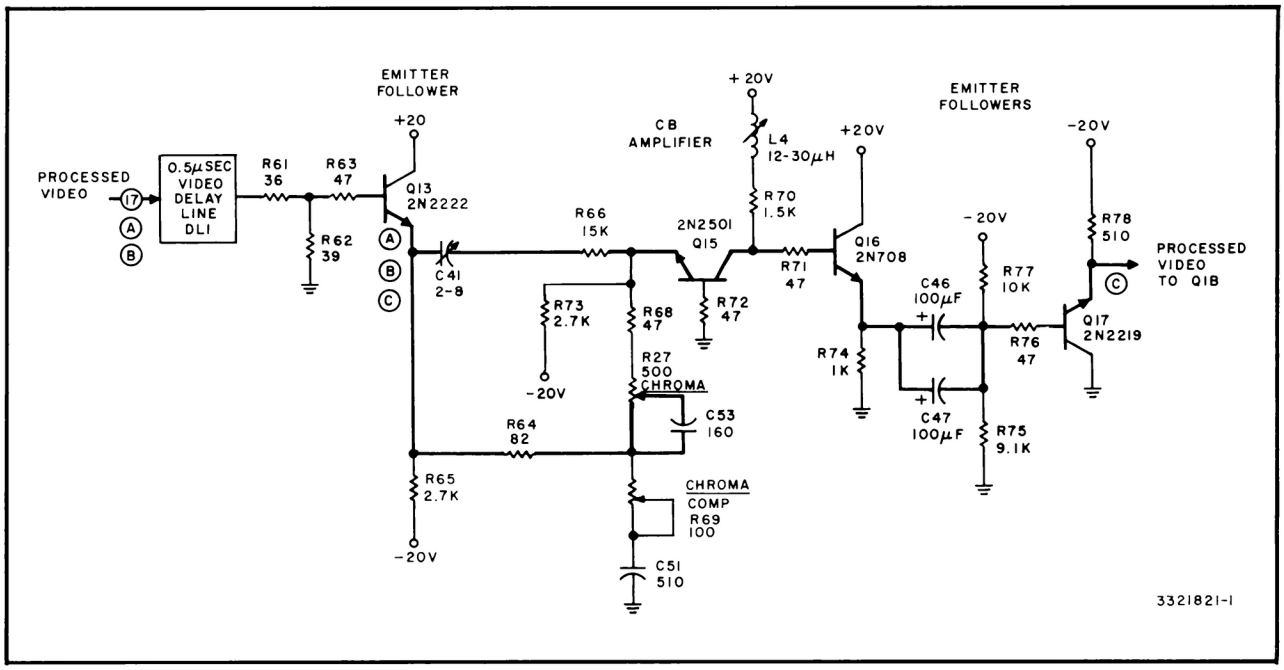
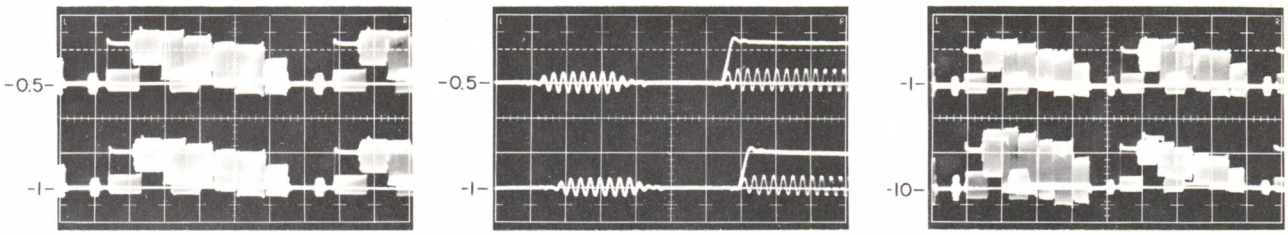


Figure 104—Video Output Module, Block Diagram





A. Top: P1-17
Bottom: Q13 emitter
Both: 1 v/cm, 10 μs/cm

B. Top: P1-17
Bottom: Q13 emitter
Both: 1 v/cm, 1 μs/cm

C. Top: Q13 emitter, 0.5 v/cm
Bot. Left: Q17 emitter (Max chroma)
Bot. Right: Q17 emitter (Max chroma)
All: 10 μs/cm

Figure 105—Video Delay and Chroma Control, Schematic Diagram and Typical Waveforms

count that the signal is fed through four cascade emitter followers (Q16, Q17, Q1 and Q2) which attenuates the signal by approximately 0.25 volt, the one volt signal must be amplified by a factor of three, which is accomplished by transistor Q15. Gain for the stage is roughly determined by the ratio of resistors R70 to R27. Therefore, for a two volt video signal at the input to the delay line, a one volt video signal is present at the output of the video line drivers.

Peaking coil L4 in the collector circuit of Q15 is adjusted to balance any distortions in the response curve at the higher frequencies. Amplified video at the collector of Q15 is fed to emitter follower Q16 which isolates the common-base amplifier Q15 from the output circuits. The output of Q16 is fed to the base circuit of emitter follower Q17. Level shifting takes place at the base of Q17 and the output at the emitter of Q17 is fed to the base circuit of Q1 (figure 105C).

Video Amplifier and Distribution

Emitter followers Q1 and Q2 form a cascade current amplifier whose output is directly coupled to three video line driver circuits. Refer to figure 107. These line drivers consist of a series amplifier and output terminating resistors that match the transmission lines fed to the external circuits. The series amplifiers are capable of driving two output lines each. The series arrangement of the transistors provides signal polarities and amplitudes such that the voltage gain of the pair is unity gain and the output impedance is low. Both ac and dc stabilization is incorporated to preserve constant levels by using voltage regulators.

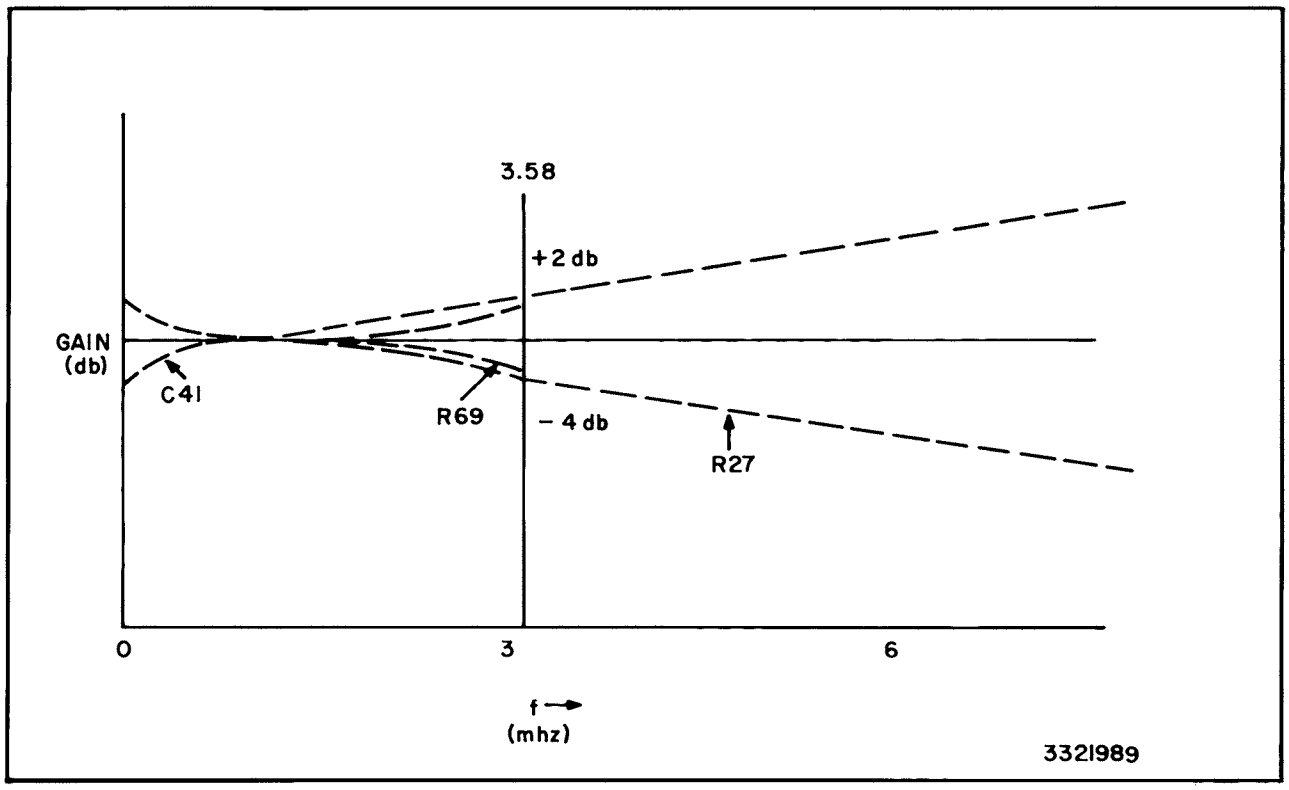


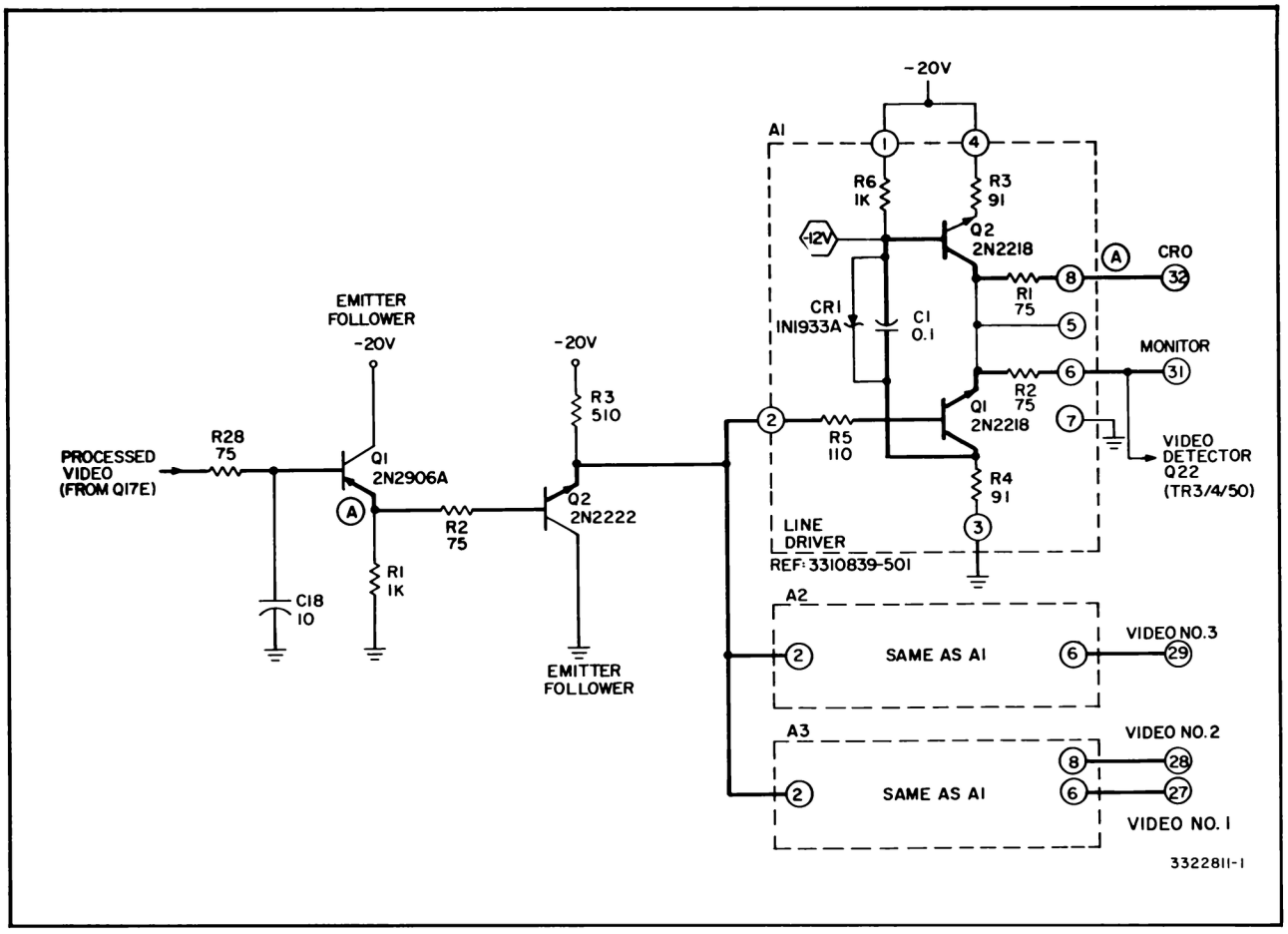
Figure 106—Chroma Response Curve

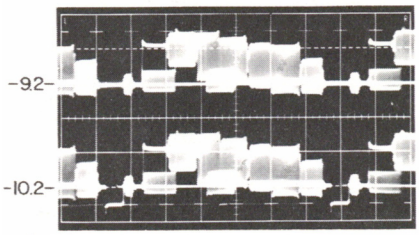
Submodule boards A1, A2 and A3 are identical and therefore function similarly. Transistors Q1 and Q2 (of the submodules) are cascaded to form a series amplifier. The collector output of Q1 is coupled to the base of Q2 through capacitor C1 and zener diode CR1. The emitter output of Q1 is combined with the collector output Q2 since both are in phase. The output level at this junction point is two volts peak-to-peak. (See figure 107A.)

Video from the line amplifiers is distributed to the following destinations. The video output signals are coupled through coupling capacitors. For the TR-22 machines the capacitors are located on the Output Coupling module H233. For the TR-3/4/50 machines the capacitors are located on the Video Processor and Video Output modules. At the junction of Q1 emitter and Q2 collector two output signals are available. One output at A1-8 (figure 107A) is fed through P1-32 to the CRO Switcher, while the second output at A1-6 is fed through P1-31 to the Monitor Switcher. The output at A2-6 is supplied through P1-29 to the video output no. 3 connector. Likewise one output at A3-8 is fed through P1-28 to the video output no. 2 connector, while the second output at A3-6 is fed through P1-27 to the video output no. 1 connector.

Sync Addition to Video Output

Referring to figure 108 regenerated sync at P1-19 from the Sync Logic module is fed to the base of transistor Q6 which is normally cut off as a result of the +0.7 volts developed by the diode CR2. At this point, since transistor Q6 is cut off, the collector potential is at −20 volts which is fed to the base of transistor Q7. In the static condition, transistor Q7 is cut off by the −20 volts on its base and therefore the emitter potential is at −20 volts. As a result of this −20 volts on the base of transistor Q8, the collector potential is determined by the level of the SYNC LEVEL potentiometer, and thus, at what ever level transistor Q5 emitter follower is operating. This voltage is approximately at −10 volts. As the negative-going edge of the regenerated sync is fed to the base of transistor Q6, Q6 conducts and its collector potential rises to −12 volts. Since the following circuit is an emitter follower, the emitter of Q7 is also at −12 volts. The positive excursion (figure 108A) is coupled to the base of transistor Q8 via trigger circuit C11 and R16 which control the speed at which transistor Q8 turns on. Transistor Q8 will remain on during the pulse duration which is approximately five microseconds. As the positive-going edge of the regenerated sync pulse is fed to the base of transistor



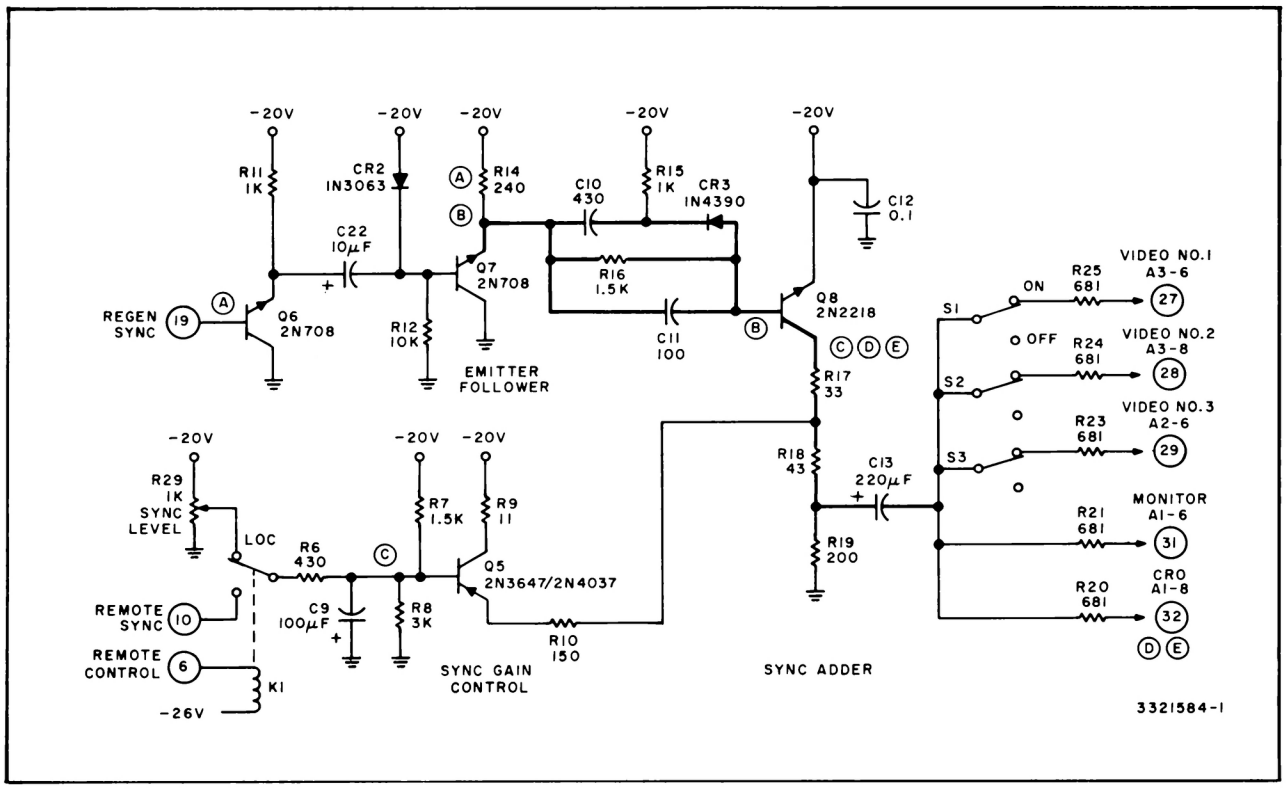


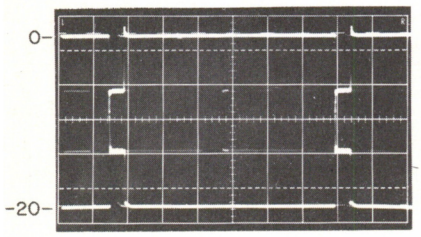
A. Top: Q1 emitter, 1 v/cm
Bottom: A1-8, 0.5 v/cm
Both: 10 μs/cm

Figure 107—Video Amplifier and Distribution, Schematic Diagram and Typical Waveforms

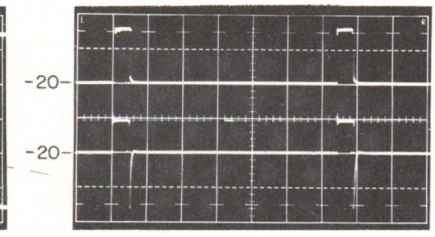
Q6, Q6 cuts off and its collector potential drops to −20 volts. Similarly, the emitter potential drops at Q7. This negative excursion is differentiated by C10 and R15 and fed to high speed switching diode CR3. The negative spike (figure 108B) passed by CR3 is fed to the base of transistor Q8 driving the transistor off, thus producing a very sharp rising edge at the collector of transistor Q8. Therefore, the two triggering circuits at the base of transistor Q8 are used to produce sharp leading and trailing sync pulse edges prior to being added to the output video. Clean, sharp, negative-going sync pulses approximately five microseconds wide and approximately 10 volts in amplitude are coupled to the video circuits via resistors R20-R25 (figure 108C). Sync pulses are added directly to the video output channels for the monitor and the CRO. The output signal at this point is approximately 0.3 volt in amplitude. This is due to both the load and source resistances being in parallel and in series with the 681 ohm resistor (figure 108D, E).

The video channels for external uses have their sync applied independently through a switch. Switch

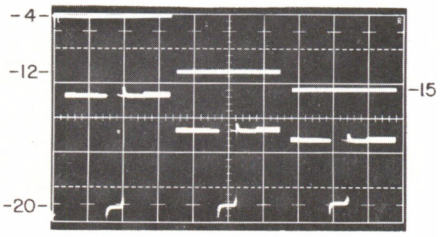




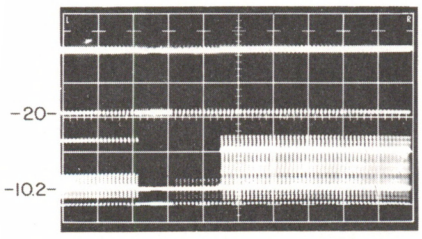
A. Top: P1-19, 2 v/cm
Bottom: Q7 emitter, 5 v/cm
Both: 10 μs/cm



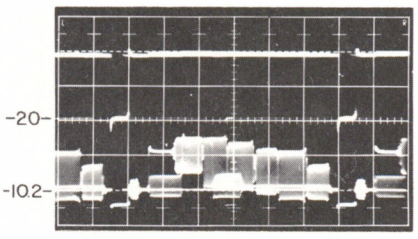
B. Top: Q7 emitter, 5 v/cm
Bottom: Q8 base, 1 v/cm
Both: 10 μs/cm



C. Top: Q5 base
Bottom: Q8 collector
Both: 5 v/cm, 10 μs/cm
SYNC Cont.: Left, Max.;
Mid, Normal; Right, Min.



D. Top: Q8 collector, 5 v/cm
Bottom: P1-32, 0.5 v/cm
Both: 500 μs/cm



E. Top: Q8 collector, 5 v/cm
Bottom: P1-32, 0.5 v/cm
Both: 10 μs/cm

Figure 108—Regenerated Sync Added to Video, Schematic Diagram and Typical Waveforms

S1 applies sync to video channel number one, and so forth. With the switch in the OFF position, the video signal is fed to the output connector without sync added. If desired, house sync may be added in an external sync adder unit.

Video Output Metering (TR-3/4/50 Only)

The purpose of the video detector circuit (figure 109) is to furnish a rectified sample of the video output to the Signal Level Meter, 4M1, on the PLAY control panel, so that the level of the outgoing video can be monitored.

A portion of the video output being fed to the CRO switcher at A1-6 is applied through coupling capacitor C56 to the base of Q22, the first of a two-stage cascade video amplifier. The amplified output on the collector of Q22 is coupled through C55 to the base of the second video amplifier, Q21. From the collector of Q21, the signal is direct coupled to the base of Q20, an emitter follower. The output on the emitter of Q20 is coupled through C54 across the input of the peak-to-peak detector which consists of CR4, CR5, and C57. Use of the emitter follower to drive the peak-to-peak detector isolates the video amplifier from the loading effects of the detector.

The rectified output of the detector is fed to a two stage video amplifier, Q24, Q23, both of which are emitter followers. The rectified signal is applied to the base of Q23 and the output on the emitter is direct coupled to the base of Q24. The meter signal is taken across potentiometer R90 in the emitter of Q24. The setting of potentiometer R90 (an internal control) determines the magnitude of the signal output current. The signal is fed via contact 3 on the B section of the AUDIO/VIDEO/CUE switch, 4S8, on the PLAY control panel, to the Signal Level Meter.

The video output level can be observed on the Signal Level Meter during playback by selecting the VIDEO position with the AUDIO/VIDEO/CUE switch. Assuming the video levels have been properly established throughout the system, the meter indicator will read zero VU for a standard 1 volt composite video output signal.

Instructions for calibrating the video level circuit of the meter are given under Adjustments.

−20 Volt Regulators

The −20 volt regulator circuit, shown in figure 110, consists of a transistor and associated circuit components. The function of the regulator circuit is to provide a regulated −20 volt dc potential to the video line drivers, to the video amplifiers and to the sync adder circuits and to the chroma circuit, while at the same time acting as a decoupling network that will prevent any current surges which may occur in the line driver circuits from excessively loading the −20 volt bus. Current required by the line drivers is supplied by the −26 volt dc supply, and the −20 volt biasing potential is obtained by the use of the −20 volt regulated bus (−20VE). The resistor R1 limits the initial current surge to the maximum dissipation rating of transistor Q. There are four similar

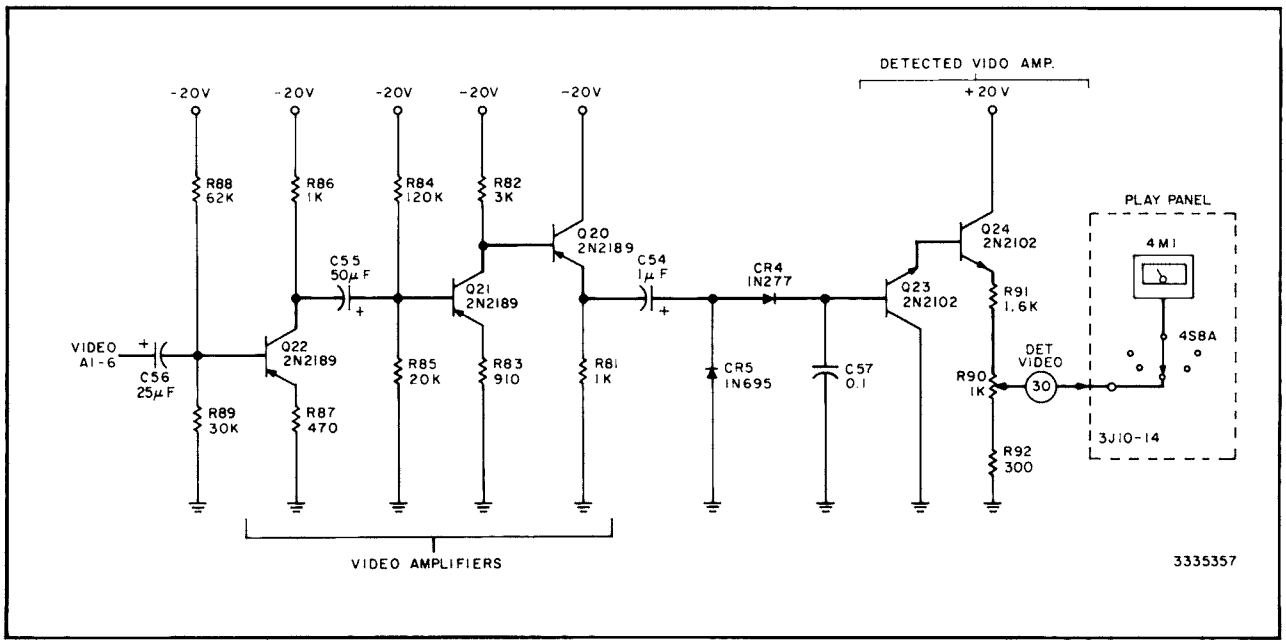
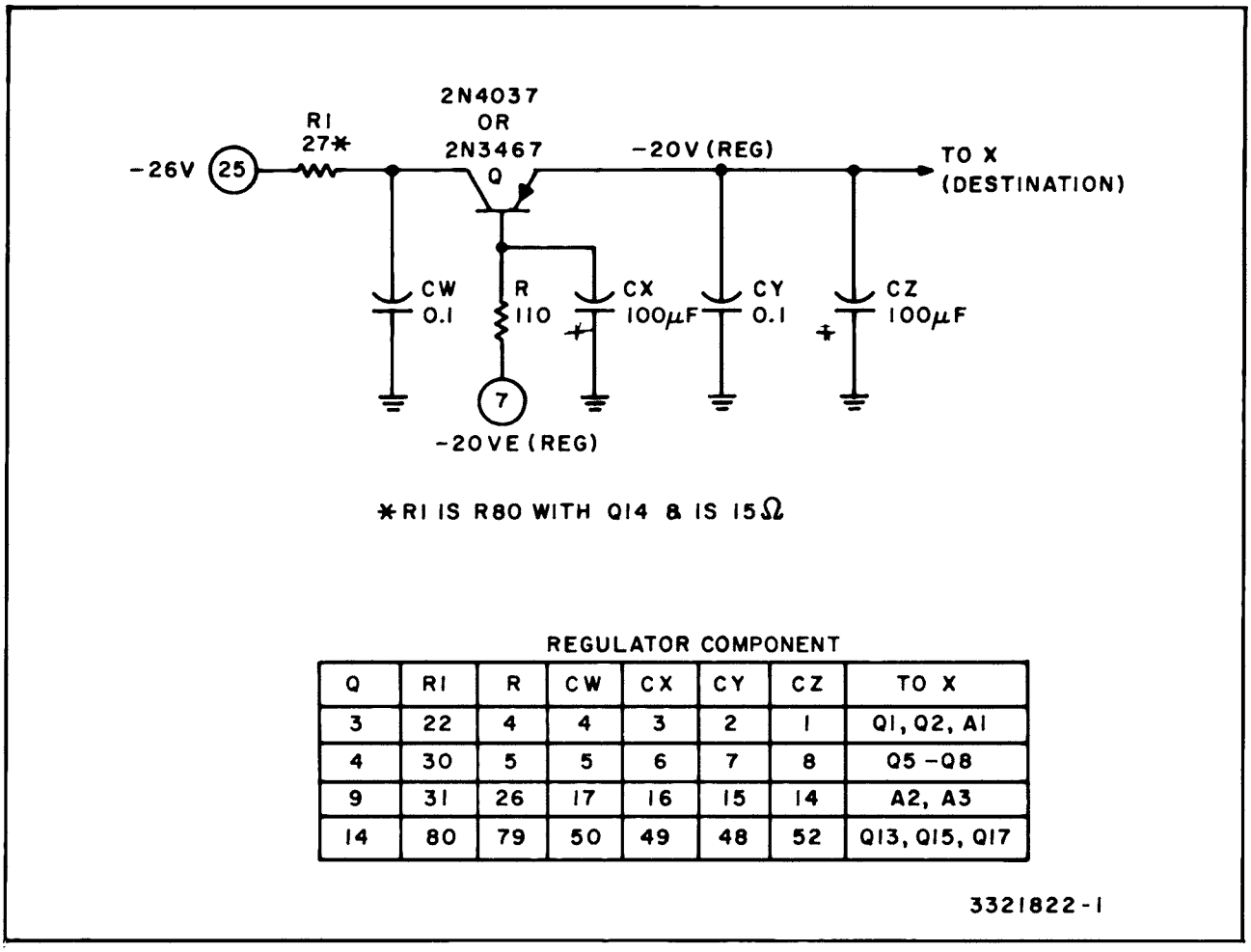


Figure 109—Video Detector (TR-3/4/50 Only), Schematic Diagram



REGULATOR COMPONENT

Q	R1	R	CW	CX	CY	CZ	TO X
3	22	4	4	3	2	1	Q1, Q2, A1
4	30	5	5	6	7	8	Q5 -Q8
9	31	26	17	16	15	14	A2, A3
14	80	79	50	49	48	52	Q13, Q15, Q17

3321822-1

Figure 110—−20 Volt Regulator

regulators on the module. Their operation is identical and therefore, the discussion will cover only one of them. A table of components is listed on the figure showing the component for each regulator circuit.

Referring to figure 110, the −20 volt regulated potential applied to the base of transistor Q biases the transistor into conduction. Therefore a potential of −20 volts appears at the emitter of Q. The potential at the emitter is then fed to the output circuits (X on the table). Since the base of Q is referenced to −20 volts, Q actually functions as a variable impedance in series with the output circuits. Thus, a potential of −20 volts is maintained at the emitter of Q regardless of normal current variation in the output circuits.

The −20 volt regulated bus is effectively isolated from the output circuits by a decoupling network consisting of a capacitor multiplier. The capacitor multiplier consists of capacitor CX and Q. The value of the equivalent filter capacitor across the −20 volt regulated supply may be calculated as follows:

$$Cd = \beta \times CX$$

Where Cd = decoupling capacitor
β = beta of transistor Q
CX = capacitor CX (microfarad)

ADJUSTMENTS

CAUTION: Some internal variable reactance and resistance components are sealed with a red compound. This indicates that it is a factory adjustment which should not be readjusted in the field. If service is required, notify the RCA field representative.

Do not adjust the following:

Capacitor C41, low frequency response

Coil L4, high frequency response

Potentiometer R69, chroma compensation

Chroma Level, R27

The chroma level control is adjusted so that the chroma portion of the video signal is at a standard

brightness with respect to the luminance portion of the video signal. Also, when the tape recorder is operated at a remote location, the chroma level, which is not variable at the remote panel, should be at or very close to unity gain.

Perform the following steps when adjusting the CHROMA level control.

1. With the tape recorder in the STOP mode, depress the H and NORM buttons on the CRO monitor and select the VID OUT signal on the CRO switches.

2. Check the luminance level (bright line which represent the white bar) for 77 IRE units. Adjust the Video Level control on the video processor module if necessary.

3. Adjust the CHROMA LEVEL control until the top of the fourth chrominance bar (magenta) is 77 IRE units.

4. Check the burst level for 40 IRE units peak-to-peak. If adjustment is necessary, use the BURST GAIN control on the front panel of the Burst processor module to correct the burst level.

Metering Circuit Signal Level

The setting of the metering circuit signal level potentiometer, R90, should not be disturbed in the course of routine maintenance. If component replacement in the video detector circuit affects the output level, or if for some other reason the meter reading is not valid, the calibration of the circuit can be checked by following the procedure below.

1. Place the equipment power circuit breaker, 1CB1, in the OFF position.

2. Mount the Video Output module in an extender and insert in the TR-4.

3. Load the TR-4 with a tape recording of a standard signal.

4. Place the equipment power circuit breaker, 1CB1, in the ON position.

5. Place the TR-4 in PLAY mode and make the required playback operation checks. (Refer to the *TR-4 Operation Manual, IB-31810.)*

6. Turn the AUDIO/VIDEO/CUE switch on the PLAY control panel to VIDEO and observe the Signal Level Meter. The indicator should read zero VU. If not adjust R90 to obtain a reading of zero VU.

7. Place the power circuit breaker in the OFF position. Remove the extender and replace the module in the TR-4.

STANDARDS GENERATOR MODULE

General

Basically, the Standards Generator module provides a group of outputs designated "standards" busses, of which one is grounded according to the standard selected. It also provides a group of busses for frequency control of the Modulator module; the active bus having a level of −20 volts. Busses representing inactive standards are open-circuited. Control logic for the Standards Generator module is described in IB-31859-1.

Machines intended for international use are equipped with five standards busses and five modulation busses. Machines intended for use with domestic or 525-line operation are equipped with only three busses for standards and three for modulation control. Table 9 lists the state of each control bus for all operating standards. Table 10 lists the state of the vertical and horizontal busses for the three common line standards. Figure 111 illustrates the function of the Standards Generator in the Playback section of the machine. Figure 112 represents the Record side of the machine.

TABLE 9—CONDITIONS OF STANDARDS BUSSES AND MODULATION CONTROL BUSSES

STANDARD SELECTED	*CONDITION OF STANDARDS BUSSES*				
	1	*2*	*3*	*4*	*5*
Std #1 405/525 LB MONO	Ground	Open	Open	Open	Open
Std #2 625* LB MONO	Open	Ground	Open	Open	Open
Std #3 LB COLOR	Open	Open	Ground	Open	Open
Std #4 405/525 HB	Open	Open	Open	Ground	Open
Std #5 625* HB	Open	Open	Open	Open	Ground
STANDARD SELECTED	*CONDITION OF MODULATION CONTROL BUSSES*				
	1	*2*	*3*	*4*	*5*
Mod #1 405/525 LB MONO	—20v	Open	Open	Open	Open
Mod #2 625* LB MONO	Open	—20v	Open	Open	Open
Mod #3 LB COLOR	Open	Open	—20v	Open	Open
Mod #4 405/525 HB	Open	Open	Open	—20v	Open
Mod #5 625* HB	Open	Open	Open	Open	—20v

* International Machines Only.

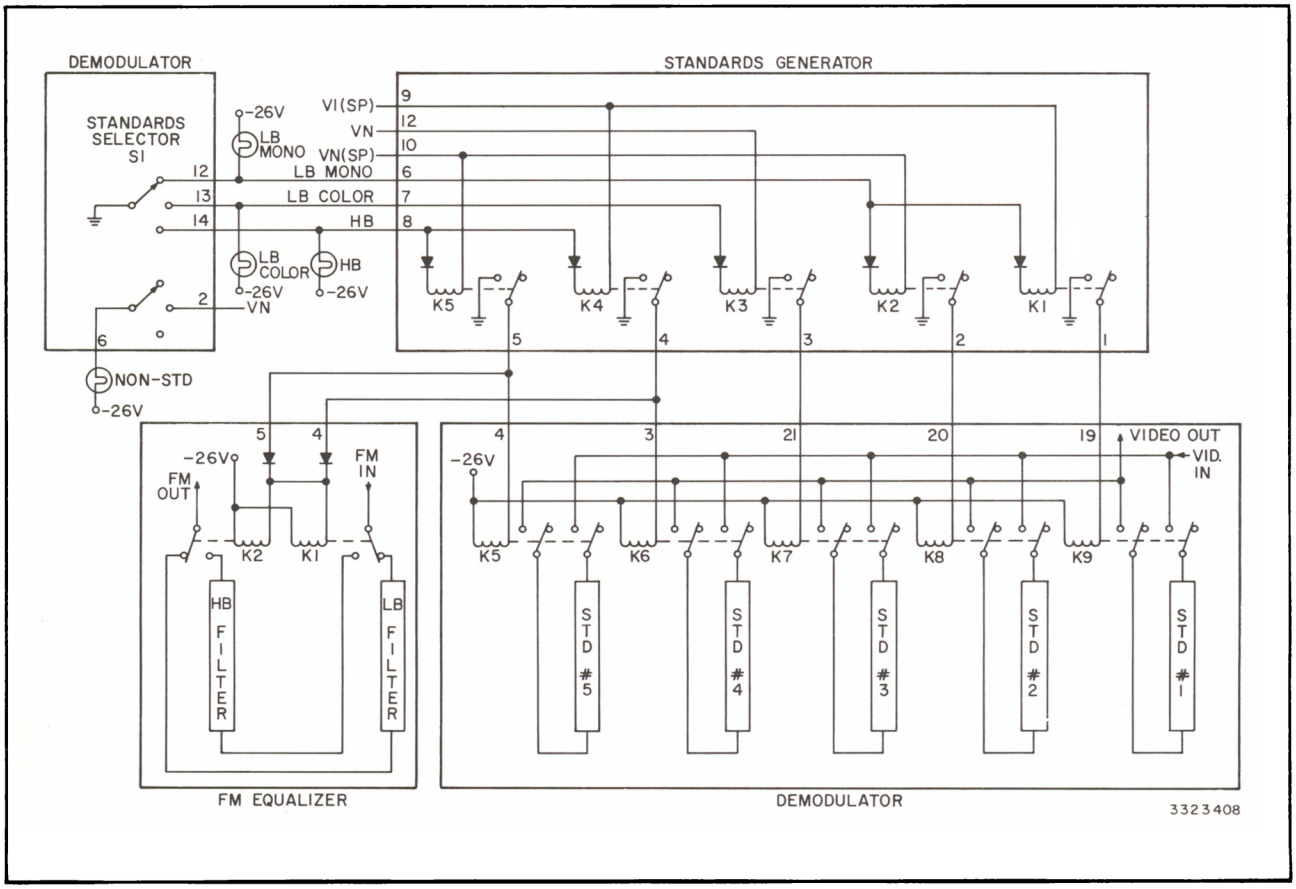


Figure 111—Standards Control During Playback

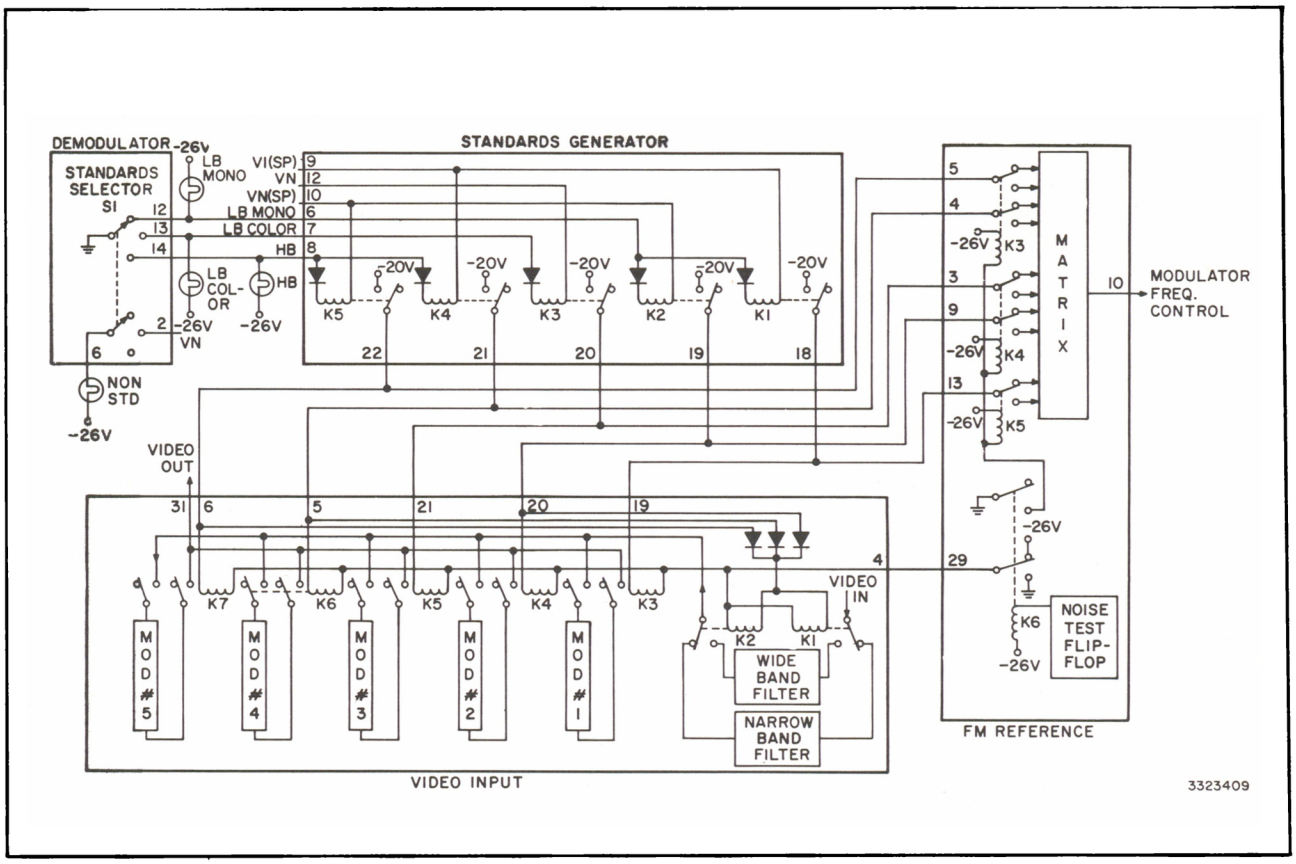


Figure 112—Standards Control During Record

TABLE 10—CONDITION OF VERTICAL AND HORIZONTAL BUSSES

BUS	*405*	*525*	*625*
HN	Ground	—20v	—20v
HI	—20v	Ground	Ground
VN	Ground	—20v	Ground
VI	—20v	Ground	—20v
VN (Special)	—20v	—20v	Ground
VI (Special)	Ground	Ground	—20v

PREAMPLIFIER FILTER MODULE

General

The Preamplifier Filter module contains five RC filters and three LC filters. These filters are used to filter dc voltage busses before entering the FM Preamplifier module. The filters also filter the control signal lines to the head switching relays in the FM Preamplifier module. Since the FM signal in this module is in the one millivolt region, the noise and/or ripple on the dc busses becomes very critical.

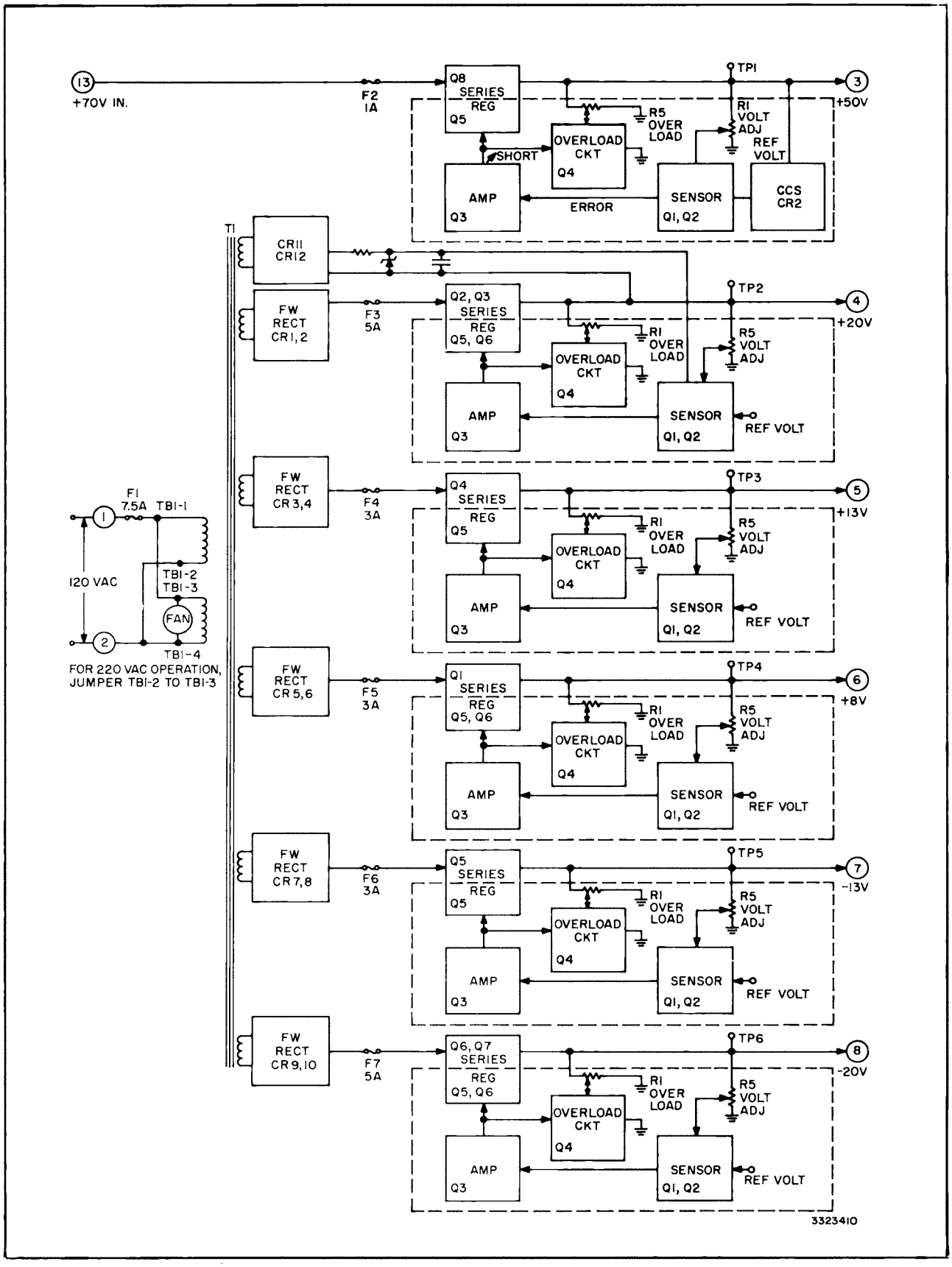


Figure 113—Auxiliary Power Supply H1A10, Block Diagram

AUXILIARY POWER SUPPLY, H1A10

CIRCUIT DESCRIPTION

General

The auxiliary power supply is located on the back of the main frame. The supply as shown on figure 113, provides six separate dc voltages which are used to assist the main dc power supply system load requirements. In addition, it supplies several dc voltages that are required to accommodate the high band circuitry. Each transformer section is individually fused to protect it. Convenient test points are provided so that during maintenance routines the dc voltages may be monitored. Voltage adjustment controls and current sensitivity controls are accessible from the front of the unit.

The distribution of dc power is available in the Diagrams manual on the DC connection, individual module schematic or harness drawings.

Six dc voltages are provided, as follows:

1. +50 volts switched @ 0.5 ampere
2. +20 volts @ 3.5 ampere
3. +13 volts @ 1.5 ampere
4. +8 volts @ 2 ampere
5. −13 volts @ 1.5 ampere
6. −20 volts @ 3.5 ampere

The +50 volt switched supply is derived from the +70 volt switched bus; whereas, all of the other supplies are derived from an ac source through fullwave rectifiers.

Figures 114 through 118 illustrate the power supply and its components. Figure 115 shows that an

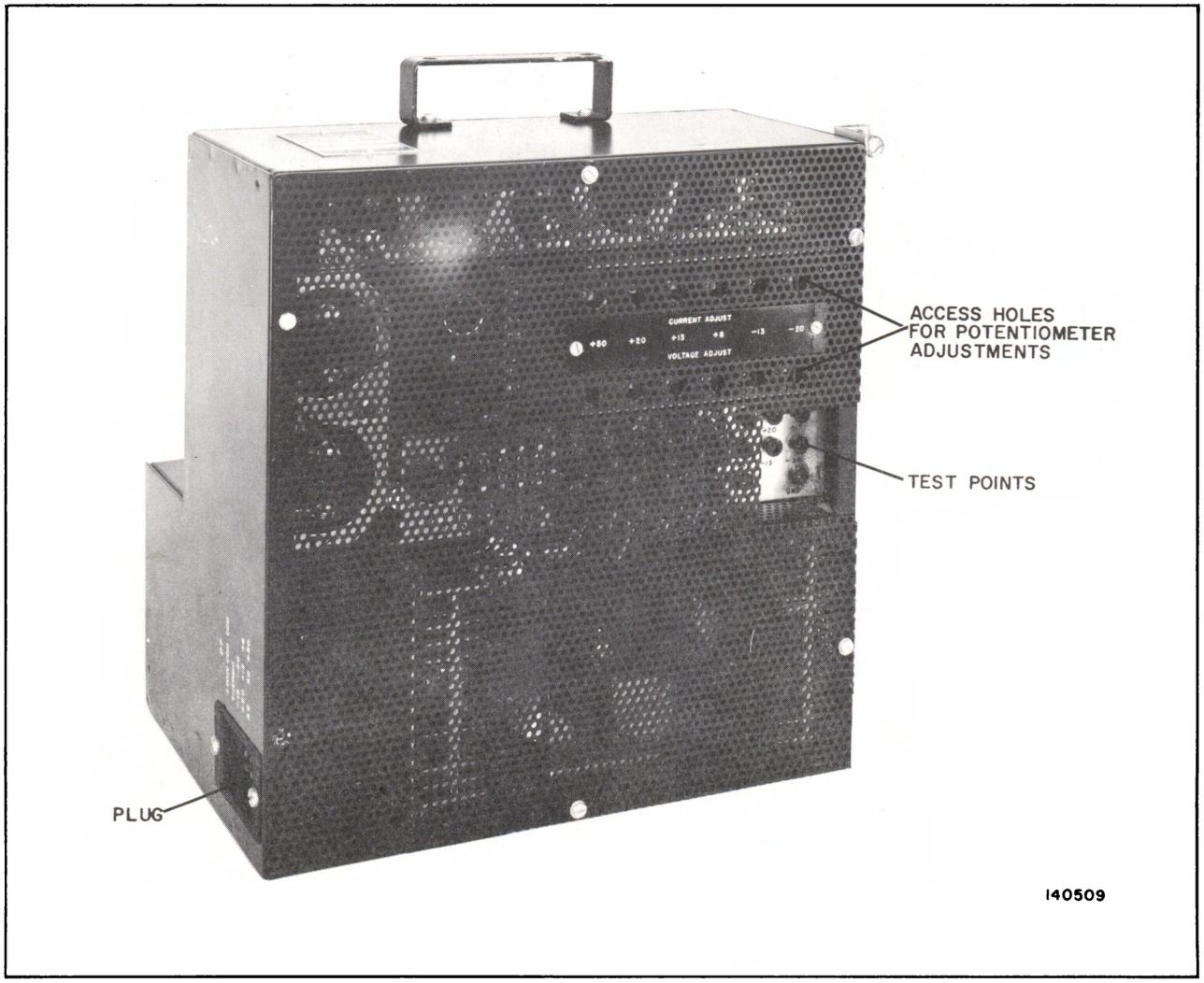


Figure 114—Front View of Auxilary Power Supply H1A10

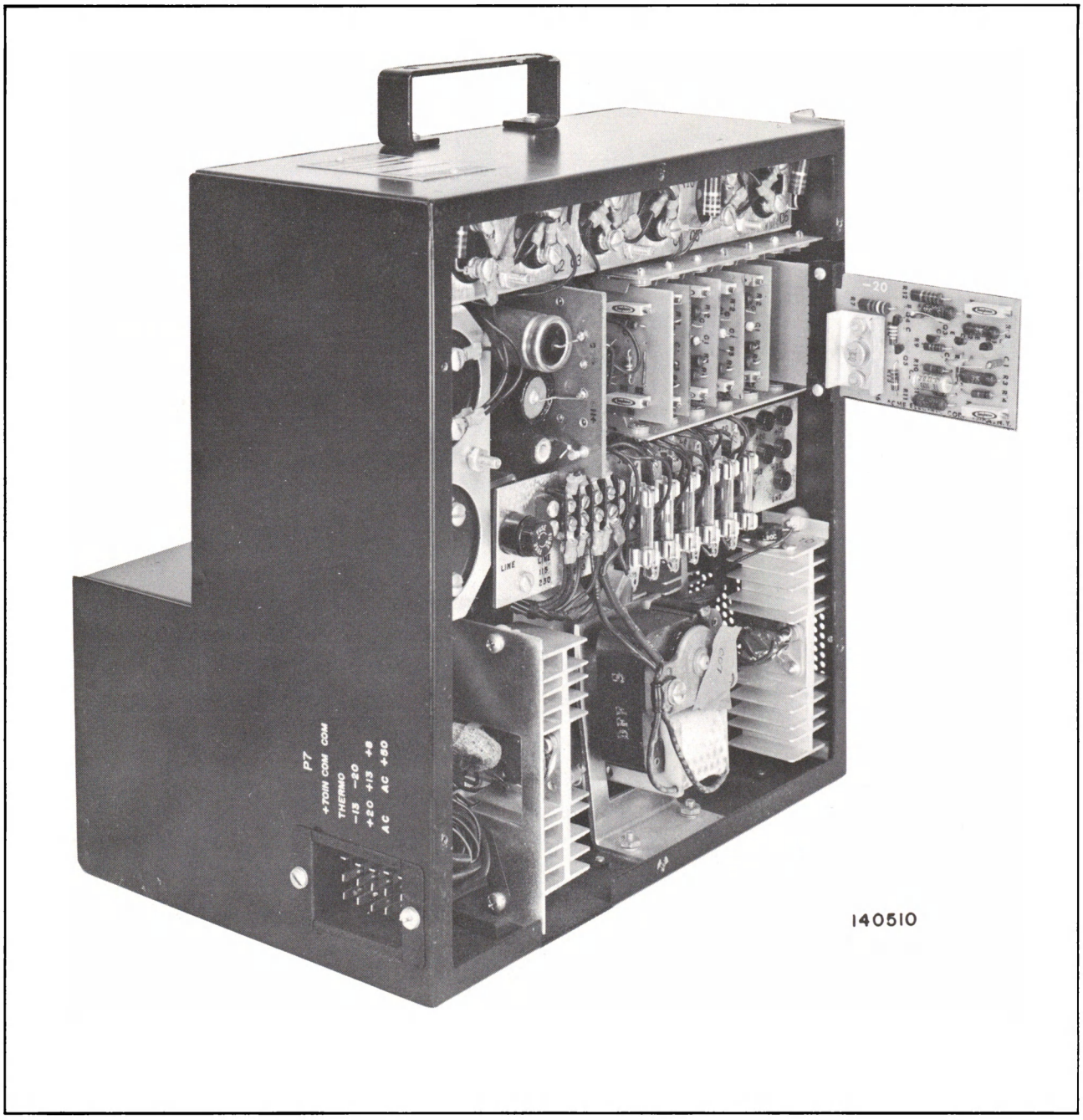


Figure 115—Front View of Auxiliary Power Supply with Regulator Board on Extender Frame

extender frame may be used to troubleshoot a regulator board while still in the circuit.

Regulator System

The six regulator circuits are all of the series regulator type but differ in detail. The basic operation of a series regulator can be explained most simply as follows:

1. A fraction of the output voltage is obtained from a precision voltage divider.

2. The output voltage sample is compared to a stable reference voltage.

3. A current proportional to the voltage difference is amplified and then fed to the base of a series regulator, which is merely dc-coupled cascaded emitter followers with the final stage connected in *series* with the input voltage and the load.

4. A potentiometer in the voltage divider across the output is used to adjust the output voltage sample to match the reference voltage at the desired output voltage.

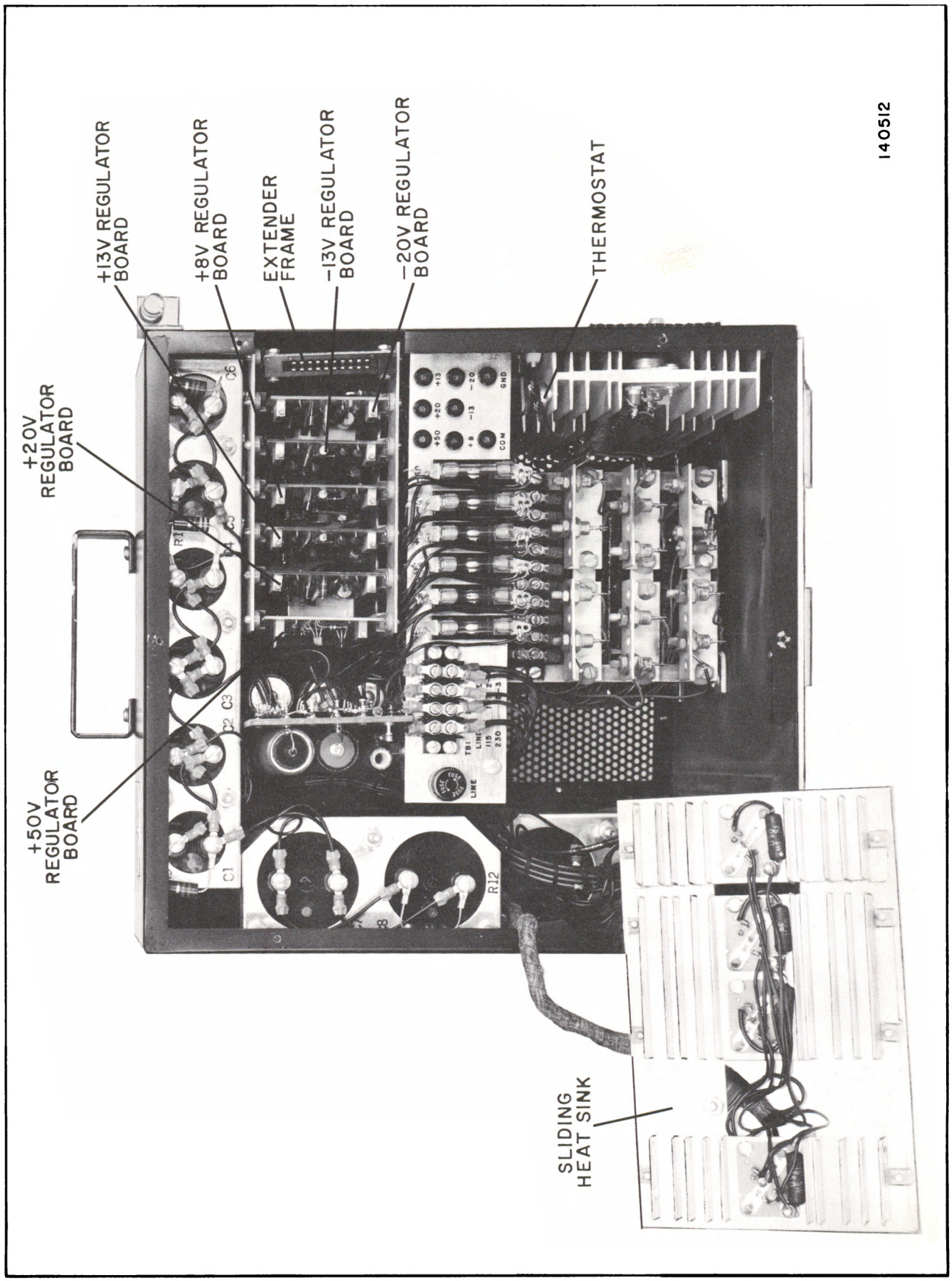


Figure 116—Front View of Auxiliary Power Supply with Fan and Sliding Heat Sink Removed

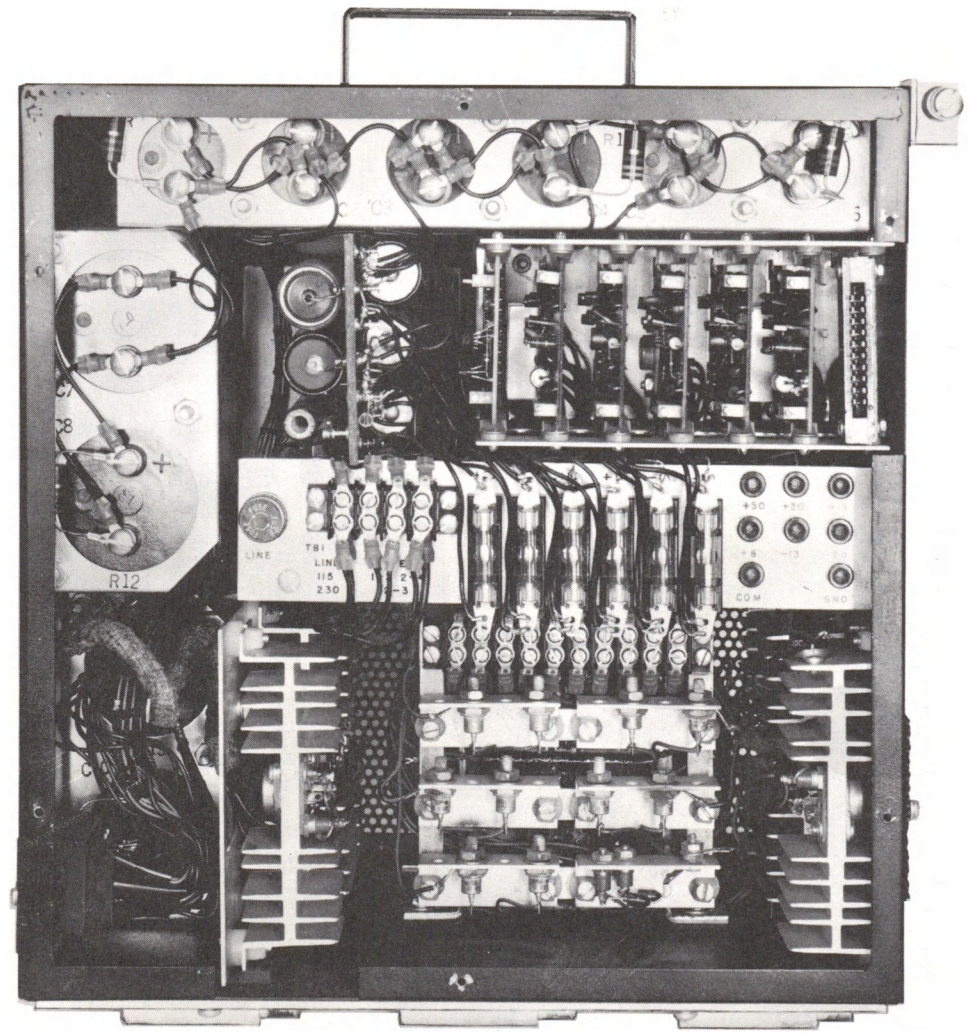


Figure 117—Front View of Auxiliary Power Supply with Fan Removed to Expose Components

5. The action of the regulator is then similar to that of a feedback amplifier. When the output voltage is correct the circuit remains in a stabilized condition. If a change in output voltage tends to occur, the amplified error signal causes the series regulator to change the output voltage in the direction that tends to minimize the error.

+50 Volt Supply

This supply obtains its input from the +70 volt switched bus. In order to protect the differential amplifier Q1-Q2 from the +70 volts; which exceeds the breakdown voltage of the transistors, Zener diode CR14 is permitted to fire when the output is at zero volts. This clamps the collector voltage at +24 volts. As the output voltage rises toward +50 volts, the difference of potential across CR14 decreases to a point where the diode is cut off. At this time, the sensing circuit is functioning and regulates the output voltages.

Zener diode CR2 provides a stable reference voltage of 41 volts at the base of Q1. This also establishes a constant current through common emitter resistor R3. A sample of the output voltage is obtained by the voltage divider, R6, potentiometer R1 and R7. Potentiometer R1 permits adjusting the output voltage sample so that the output stabilizes at +50 volts.

A small change in the sample voltage provides a large change in correction voltage which is further

amplified by transistor Q3. Transistor Q3 amplifies the difference in the collector potentials of Q1 and Q2. The output of Q3 is fed directly to the base of transistor Q5. Q5 and Q8 form the cascaded emitter follower series regulator. Q8 is known as the path transistor, since it is directly in the path of the output. Q8 can also be analyzed as a variable resistance in the output path which is modulated by the error signal. Any fluctuation in output voltage will cause a resultant change that alters the output voltage in the direction that tends to minimize the error.

Potentiometer R5 adjusts the point at which the overload circuit activates and diverts the current, being supplied to Q5, through Q4 to ground. The voltage at the output drops, since the series regulator is disabled, and falls toward zero. Zener diode CR14 prevents the +70 volt input from appearing across the differential amplifier, it has a breakdown voltage in the 40 volt range.

Theoretically, under normally operating conditions the nominal current supplied by the +50 volt

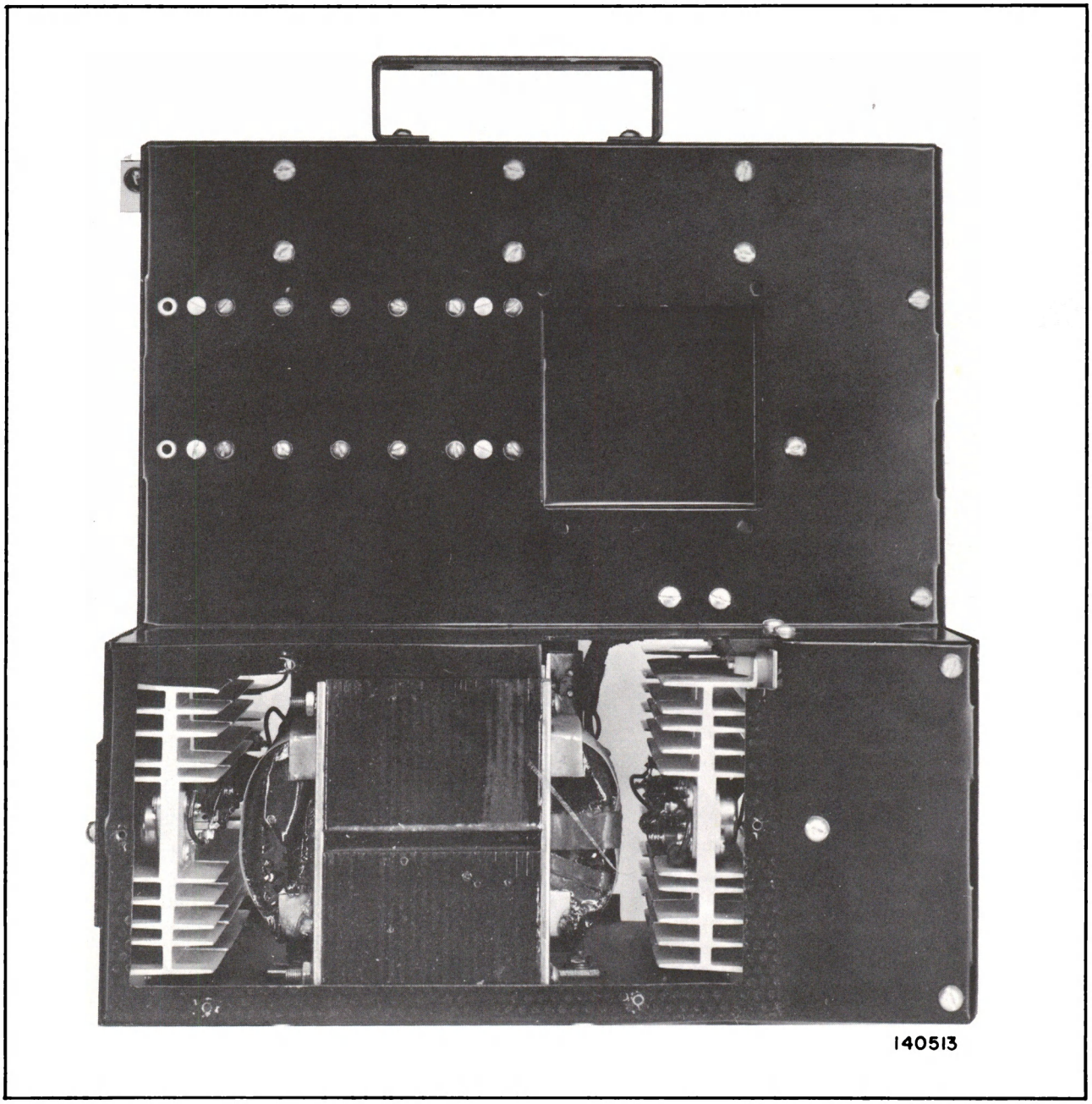


Figure 118—Rear View of Auxiliary Power Supply with Grille Removed

supply is 0.5 ampere. Thus the drop across resistor R8 is 0.75 volt. Consider a voltage drop of 1 volt between the emitter & base junction of Q8, therefore, the total voltage drop from the emitter of Q5 (also the base of Q8) is 1.75 volts greater than the output voltage.

With these values in mind, the overload potentiometer, R5, is adjusted so that when the load increases beyond the designed limit, Q4 turns on and diverts the control current through transistor Q4, which limits the series regulator transistors Q5 and Q8. The amount of control current is very small and therefore will not burn out Q4.

+20 Volt Supply

The +20 volt supply consists of a fullwave rectifier, diodes CR1 and CR2, and a filter network. The filtered dc is fed through a fuse, F3, to the +20 volt regulator. The regulator functions similarly to that of the +50 volt supply, except in small details.

Output voltage sampling is provided by voltage divider resistors R2 and R8 to the base of transistor Q2. The reference voltage is provided by the Zener diode CR1 in parallel with the voltage divider R4 and potentiometer R5. R5 permits adjustment of the operating point of the differential amplifier, Q1-Q2, and also adjusts the output voltage to the correct level. Zener diode CR13 provides a reference voltage of +28 volts for the collectors of Q1-Q2.

Transistor Q3 amplifies the difference voltage resulting from an unbalanced output voltage and feeds the error correction signal to Q5 and then to Q6. Transistors Q5 and Q6 are needed because of the amount of current being handled by this supply. This same reason is behind the use of transistors Q2 and Q3 in the path of the output voltage.

Overload protection is accomplished in the same manner as previously described for the +50 volt supply.

+13 Volt Supply

The +13 volt supply consists of a fullwave rectifier, diodes CR3 and CR4, and a filter network. The filtered dc is fed through a fuse, F4, to the +13 volt regulator. The regulator functions similarly to that of the +20 volt supply, except for voltage differences. Collector supply for Q1-Q2 is supplied by the +20 volt bus.

Overload protection is accomplished in the same manner as previously described for the +50 volt supply.

+8 Volt Supply

The +8 volt supply consists of a fullwave rectifier, diodes CR5 and CR6, and a filter network. The filtered dc is fed through a fuse, F5, to the +8 volt regulator. The regulator functions similarly to that of the +20 volt supply, except for voltage differences. Collector supply for Q1-Q2 is supplied by the +20 volt bus.

Overload protection is accomplished in the same manner as previously described for the +50 volt supply.

−13 Volt Supply

The −13 volt supply consists of a fullwave rectifier, CR7 and CR8, and a filter network. The filtered dc is fed through a fuse, F6, to the −13 volt regulator. The regulator functions similarly to that of the +20 volt regulator, except for voltage differences. Collector supply for Q1-Q2 is supplied by the +8 volt bus.

Overload protection is accomplished in the same manner as previously described for the +50 volt supply.

−20 Volt Supply

The −20 volt supply consists of a fullwave rectifier, CR9 and CR10, and a filter network. The filtered dc is fed through a fuse, F7, to the −20 volt regulator. The regulator functions similarly to that of the +20 volt regulator, except for voltage differences. Collector supply for Q1-Q2 is supplied by the +8 volt bus.

Overload protection is accomplished in the same manner as previously described for the +50 volt supply.

REGULATOR MODULE

CIRCUIT DESCRIPTION

General

The Regulator module used in the TR-22HB machines is covered in the *Control and Power Supply Systems* maintenance manual, IB-31623-1.

The Regulator module used in the TR-3/4/50 machines as shown on the block diagram, figure 119, contains the following circuits.

1. +70 volt regulator
2. −10 volt regulator
3. −20 volt regulator
4. +13 volts switched
5. +70 volts switched

The three regulator circuits are all of the series regulator type but differ in details. The basic operation of a series regulator can be explained most simply as follows:

1. A fraction of the output voltage is obtained from a precision voltage divider.

2. The output voltage sample is subtracted from a stable reference voltage. The subtraction may be performed either by a common-emitter stage or by an emitter-coupled differential amplifier.

3. A current proportional to the voltage difference is amplified and then fed to the base of a series regulator, which is merely dc-coupled cascaded emitter followers with the final stage connected in *series* with the input voltage and the load.

4. A potentiometer may be inserted in the sampling voltage divider across the output to adjust the output voltage sampling to match the reference voltage at the desired output voltage.

5. The action of the regulator is then similar to that of a feedback amplifier. When the output voltage is correct the circuit remains in a stabilized condition. If any change in the output voltage tends to occur the amplified error signal causes the series regulator to change the output voltage in the direction that tends to minimize the error.

+13 Volts Switched

In the playback mode the switched +13 volts is supplied to the Preamplifier Filter module where it is filtered and then fed to the collector supply of the feedback amplifiers in the Playback Amplifier modules. In all other modes the playback amplifier supply potential, +13 volts, is switched off. Therefore, any stray noise or crosstalk from the record heads is not amplified by the Playback Amplifier modules.

+70 Volts Switched

In the record or set up mode the switched +70 volts is supplied to the switching gates in the FM Switcher module where it turns on a diode and diverts the FM signal to ground. Whereas, in the playback mode the diode is cut off and the FM signal is allowed to pass through the head resonance equalizer circuits on the FM Equalizer module.

In the record or set up mode the switched +70 volts is also supplied to the switchlock detect or circuit on the Splice Logic module where it acts as an input to an AND gate which indicates that the machine is in the switchlock servo mode so that a splice may be made.

+70 Volts Regulator

The +70 volt regulator consists of Q7 as the reference amplifier, Q4 and Q5 as the cascaded emitter followers, and Q6 as the series a regulator. A sample of the +70 volt output, for comparison with the reference voltage at the emitter of Q7 (ground in this case), is obtained from the voltage divider R9 and R10. Any change in output voltage is immediately sensed and a correction current is supplied to the series regulator in such a manner as to maintain the output at +70 volts. The +70 volt regulator has a maximum output current capability of two amperes and the output voltage from no load to full load is not less than 69 volts.

Should an overload occur, this circuit is protected by two devices, the Zener diode CR1 and the fuse F1. Zener diode CR1 will breakdown as soon as the voltage across it exceeds 33 volts. This provides an alternate parallel path for the current through the series regulator transistor Q6, thereby protecting Q6 until the fuse opens and removes the load.

−10 Volts Regulator

The −10 volt regulator consists of Q12 as a reference amplifier, two cascaded emitter followers, Q10 and Q11, and a series regulator Q9. The −26 volt input to Q9 is obtained from the −26 volt supply (special output) through a 5-ohm 160 watt resistor which protects the regulator circuit against shorts.

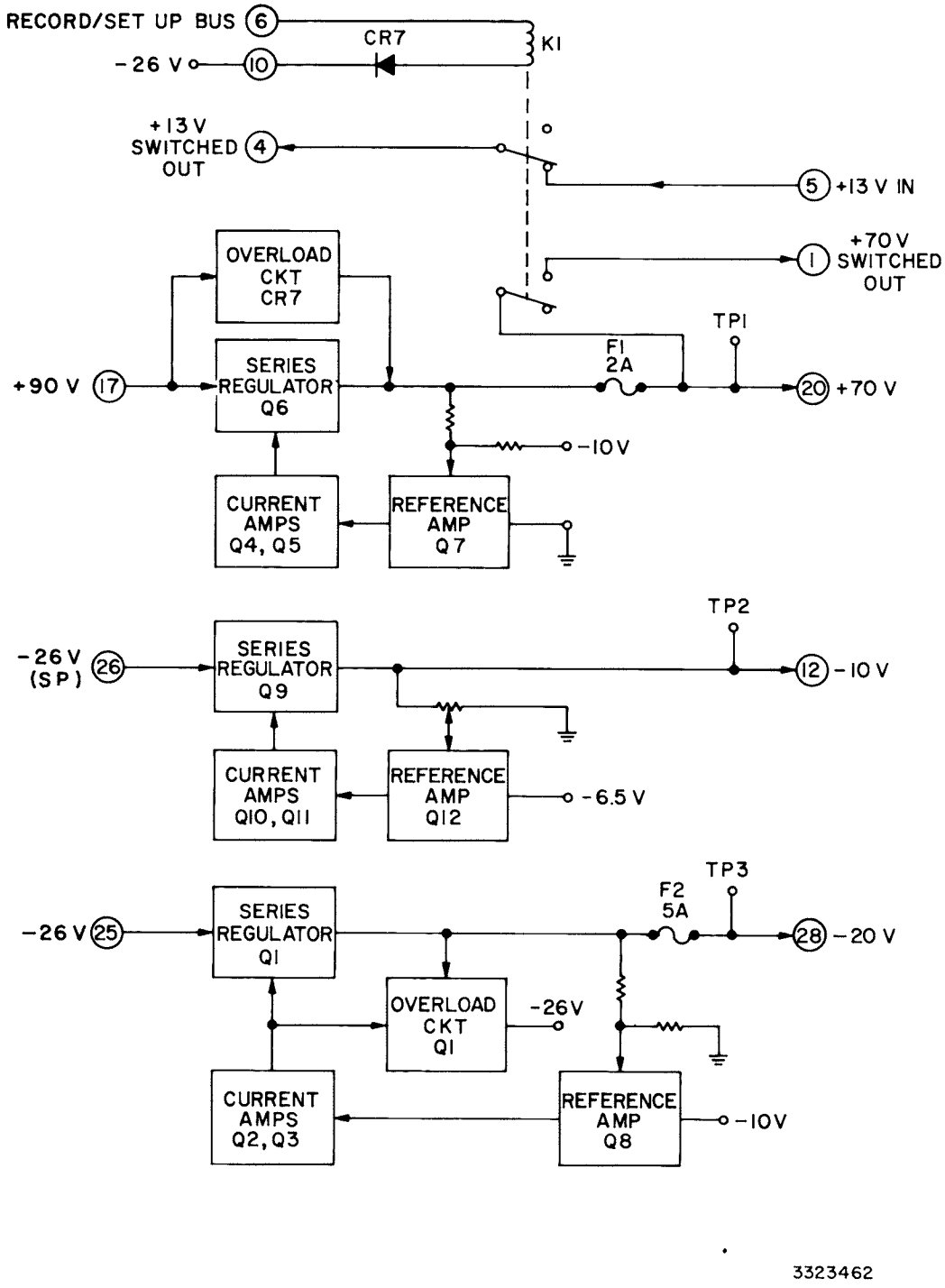


Figure 119—Regulator Module, Block Diagram

The −26 volts for Q10, Q11 and Q12 is obtained from the −26 volt bus. Zener diode CR2 in the emitter circuit of Q12 provides a stable reference voltage. A sample of the output voltage, for comparison with the reference voltage (−6.5 volts in this case) is obtained from voltage divider R20, R21 and R21 and R22. R21 is a potentiometer which permits adjusting the output voltage sample so that the output stabilizes at −10 volts. Since the −10 volt output is also used as the voltage reference for the −20 volt regulator, R21 also adjusts the −20 volt regulator.

The −10 volt regulator has a maximum output current capability of two amperes. The output voltage does not drop below −9.9 volts between no load and full load conditions.

If the −10 volt bus is shorted, Q9 becomes saturated, full voltage is dropped across the 5-ohm resistor in the output of the −26 volt supply, and the output voltage drops to zero. Subsequent removal of the short will restore operation unless the circuit breaker in the −26 volt supply is tripped. If the breaker trips, the unit will not operate until the condition is corrected and the circuit breaker is reset.

—20 Volts Regulator

The −20 volt regulator consists of reference amplifier, Q8, two cascaded emitter followers, Q2 and Q3, and a series regulator, Q1. Transistor Q13 is used to provide short circuit protection instead of a current limiting resistor.

Regulation of the −20 volt bus is similar to the −10 volt bus, except that the −10 volt regulator output is used as the reference voltage source instead of a Zener diode. The output current capability of this circuit is five amperes, and the output voltage does not drop below −19.9 volts from no load to full load.

If a short circuit occurs, the voltage drop across the 0.1-ohm resistor R32 in the emitter-base circuit of Q13 causes Q13 to conduct and rapidly supply additional current to the base of Q3. The increase in base current limits the output current while the increased current trips the circuit breaker in the −26 volt bus. Essentially the increased load current is diverted to the −26 volt bus. Thus, Q13 protects the regulator during the period between the occurrence of the short and the tripping of the circuit breaker or opening of fuse F2. The unit will not operate if the circuit breaker is open.

RCA Commercial Electronic Systems Division

Commercial Electronic Systems Division/Front and Cooper Streets/Camden, New Jersey, U.S.A., 08102

PRINTED IN U.S.A.